Section II - Poster Papers

Chairmen: Discussion Sessions

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THE TRANSPUTER BASED CCD CONTROLLER AT ESO

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ABSTRACT: A new controller concept based on transputer modules (TRAMs) and Digital Signal Processors (DSPs) has been developed at ESO. The Array Control Electronics (ACE) can handle single CCDs or CCD mosaics with 1 to 64 outputs and with up to 256 clocks with software programmable independent high and low voltages. The same basic concept will be used for slow scan scientific and fast scan auto guiding/wave front sensing applications. While the transputers are mainly used for data acquisition, communication and supervisory tasks, a DSP with very simple external logic performs the time-critical CCD clock pattern generation. The low noise, high speed clock driver with built-in telemetry is designed for highest operational safety. A newly designed video processor board has four video channels each with its own 16-bit ADC. ACE can easily be interfaced to various types of host computers like PCs, Unix workstations or ESO's VME-based LCUs (Local Control Units with VxWorks real-time operating system).

1. KEY FEATURES

ACE is host independent and works with PCs, workstations or VME systems. It has a multi-transputer controller and a DSP-based sequencer with reduced complexity. The DSP acts both as a co-processor for CCD timing and CCD Hardware control (DAC setup, gain switching, Shutter control). The hardware structure allows for multiple windowed readout with individual gain settings for each window. The system is built around classical microprocessor bus structure (ACEbus). The bus does not carry any CCD specific signals. The ACEbus is based on a standard VMEbus P1 backplane. No firmware, Transputer and DSP programs and CCD clock patterns are loaded from the host disk. There is an Electronic ID for each board with I2C-bus EEPROMs. The modular concept allows growth with detector arrays. The same concept supports technical applications (auto guiding, wave front sensing) by exchanging the video board. There are up to 256 (384 planned) clock phases per system and 4 - 64 video channels with separate ADCs. The data rate to the host is 1.6 MBytes/sec per transputer link (up to 25 MBytes/sec total). The power consumption is low, 25 watts for a single CCD. The system is safe, operating from 24 V DC. It is of compact size, (standard configuration) 150 x 150 x 300 mm³ + two VME slots.

2. SEQUENCER/CONTROLLER

The sequencer/controller is a T805 with four MByte RAM. A T225 is interfaced to a 20 MHz DSP56001 with 96 KByte RAM (commercial product from Perimos, Germany). Buffered DSP data, address and control pins are available on the bus backplane. The DSP wait state logic is in one 44-pin MACH PLD and is integrated in a RS-422 interface for the host link. A single high precision (25 ppm) clock generator (5, 8, 10, 20, 40 MHz) eight opto-isolated inputs and

outputs for shutter control and external synchronization. The I2C-bus controller is an IC (Philips PCD8584).

3. DC AND CLOCK DRIVER BOARD

There are eight DC outputs: four unipolar (0 V..25.5 V) and four bipolar (-12.8 V..+12.7 V). There are 16 bipolar clock outputs (-12.8 V..+12.7 V). Each output has its own eight-bit DAC (40 DACs in five ICs in total). Reference voltages (0, 1, 10 V) are software selectable. The driver can be turned off under software control for "on-the-fly" CCD change. No transients appear on the CCD lines during power-up (typical less than 100 mV). There are fast and equal (!) rise and fall times (typical 5 ns for 10 V amplitude). A built-in, 32 channel telemetry with a dedicated 12-bit ADC is connected directly to the DC and clock outputs. A hardware selectable board has addresses (0 - 15); 16 boards are individually addressable. In software selectable address mode (0 - 3) up to four boards can be cascaded to generate 64 independent clocks; up to 16 boards can operate in parallel.

4. 16/20-BIT VIDEO PROCESSOR

There area four channels with separate 16-bit ADCs (Crystal CS5101A). Data acquisition is done with a T225 transputer. The instrumentation amplifier input has software programmable gain. There is DC restoration with pixel clamp and a CDS with proven dual slope integrator design. The ADC offset is directly fed into the integrator. No extra opamp stage is required! A special 20-bit mode has two integrators in parallel with different time constants per channel connected to the two ADC inputs. The time penalty is only 2.5 sec for a 1024 x 1024 quad readout CCD. The video gain range is 1 - 128 in eight steps (1,2,4,..,128). There is an integrated RS-422 interface for an optional data link. A hardware selectable board has addresses (0..15); 16 boards are individually addressable. Under software address modes (0..3) are selectable; four groups of CDS timing are possible. There is an I2C-bus EEPROM for identification and/or setup storage.

5. AUXILIARY FUNCTIONS BOARD

This board contains shutter and temperature control with a dedicated transputer. There is temperature control with a digital control loop via 16-bit DAC and ADC. Four channels measure temperatures with telemetry readout and direct readout via voltmeter.

6. POWER SUPPLY

DC/DC converters generate all the necessary supply voltages (+5 V, ±15 V, +30 V) from a 24 V input. There is a common mode for input filters and a differential mode for output filters. There is a controlled power-up and power-down sequence and a voltage supervisory circuit with "power good" output.

7. FUTURE PLANS

We plan to expand the clock driver to 24 clocks per board. We will use faster DSP (56002) with 40 MHz, a single fiber link for multiple (four) transputer links using the TAXI chip set and a Local transputer graphics board for real-time display.