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A 28-nm E-band low noise amplifier with minimum 3.8 dB noise figure

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Research Paper

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Abstract

This paper presents a three-stage E-band low-noise amplifier (LNA) fabricated in a 28-nm Complementary Metal Oxide Semiconductor High-Performance Compact Plus process. The proposed E-band LNA achieves a peak gain of 16.8 dB, exhibiting a gain variation of less than ±0.5 dB across the frequency range of 67.8–90.4 GHz. The measured 3-dB gain bandwidth spans from 64 to 93.8 GHz, and the minimum measured noise figure (NF) is 3.8 dB. By employing a one-stage common-source with a two-stage cascode topology, the proposed E-band LNA demonstrates competitiveness in terms of gain flatness and NF when compared to recently published E-band CMOS LNAs.

Introduction

The 71–76 and 81–86 GHz bands (called E-bands, covering 60–90 GHz) are allowed for global wireless communications. These 10 GHz bands provide opportunities for achieving higher data rates that are not feasible in lower microwave bands. For E-band receivers, a wideband low-noise amplifier (LNA) with high gain and low noise figure (NF) is required to minimize the NF across the Rx chain and to compensate for conversion losses and the following down-converted high-noise mixer.

In general, III–V compound semiconductor technology is preferred to be used for E-band LNAs, which has better noise performance and efficiency than CMOS. Nevertheless, there are still many attempts to adopt CMOS technology to the E-band range due to its low cost and high integration advantages, and there are already plenty of successful researches in CMOS E-band LNAs [1–8].

Circuit design

There are three key points that should be considered for conventional LNA design. The first point is gain performance, the second is noise performance, and the third is stability. Additionally, the gain flatness of the LNA used for astronomical reception is also important as it affects the sensitivity and the channel capacity when integrating the LNA into a receiver system.

From Table 1 [6], it is observed that the two-stage common-source (CS) followed by one-stage cascode topology provides excellent minimum noise performance and wide bandwidth. Reference [3] uses three cascode stages, which offers high gain performance while maintaining good noise performance, but it has a narrower bandwidth and insufficient linearity. On the other hand, reference [1] employs four CS stages, resulting in the widest bandwidth and good linearity. However, it has slightly higher noise performance and may occupy a larger chip area. Considering the trade-off between CS and cascode topologies mentioned above, the proposed amplifier adopts a one-stage CS followed by a two-stage cascode configuration to achieve low noise and high gain performance. Figure 1 shows the circuit schematic of the proposed E-band three-stage LNA. The design details of this E-band LNA are further explained in the following subsections.

Circuit architecture

From Friis formula for noise, it is known that front stages of the design will dominate the overall noise performance. Thus, in the first stage, CS topology is selected to improve the noise performance. In the second and third stages, a cascode topology with gm-boosting transmission line [9, 10] and noise reduction transmission line (TL_{12}) [2, 11] techniques is selected to achieve high gain while not sacrificing too much noise performance, as shown in Fig. 2.

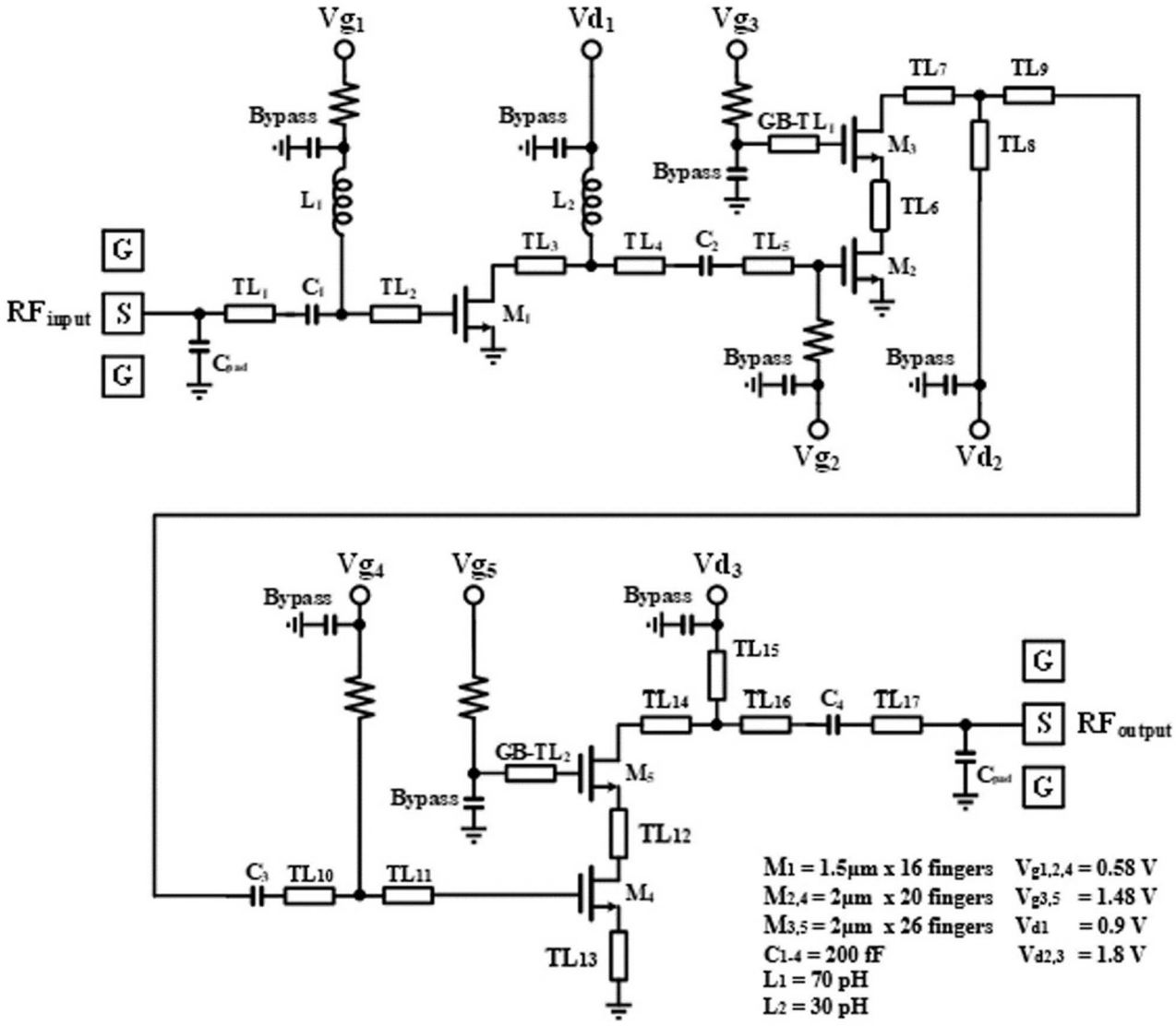

Figure 1. Circuit schematic of the proposed E-band LNA. (one-stage common-source + two-stage cascode).

Traditionally, the use of a differential pair with a neutralized capacitor topology is preferred over a single-ended topology. A differential pair offers excellent common-mode noise rejection of the supply voltage. Additionally, for high-frequency circuits, the grounding issue poses a significant challenge, which can be easily addressed by employing the virtual ground of a differential circuit. Several studies have demonstrated excellent performance of differential pairs in the E-band. However, a major concern arises from the large loss introduced by the input balun, which may be a challenge for achieving low NF performance. In reference [7], an input transformer causes a loss of 1.5–2.1 dB across the designed frequency range, making it difficult to achieve low NF performance. In reference [12], the NF performance with a balun is approximately 1.5 dB higher compared to without a balun.

In reference [10], a comparison of single-ended configurations between CS and cascode topologies reveals that the CS topology is known for its superior noise performance but compromises gain and isolation, whereas the cascode topology offers higher gain and isolation but typically exhibits worse noise performance. Therefore, in this work, a single-ended topology with a cascode configuration following the CS topology is adopted. This approach helps mitigate the significant loss introduced by the input balun and also leads to a better NF. Figure 3 demonstrates the input matching S-parameter of the proposed LNA, where a loss of 1.1 dB is achieved at the center frequency.

Device and bias selection

The bias conditions and device sizes should be determined first to optimize the performance of the LNA. For the selection of bias, V_D is chosen at 0.9 V/1.8 V for CS/cascode stage of the LNA to obtain maximum gain for 28-nm CMOS HPC-plus process.

On the other hand, the transconductance of the device reaches its maximum value at V_G of 0.8 V, which is the class-A operation. However, LNAs are often operated at small-signal region. Thus, the bias voltage of the LNA can be operated at lower voltage (about 0.6–0.7 V). Under these bias ranges, the gain performance

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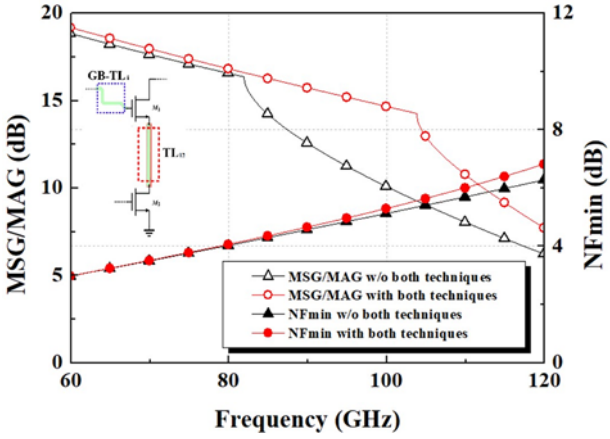

Figure 2. Comparison of the MSG/MAG and NF_{min} of a cascode stage with both noise reduction and gm-boosting techniques.

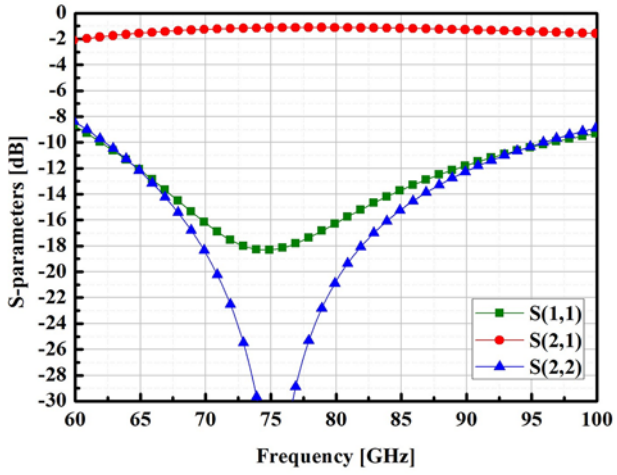

Figure 3. The input matching S-parameter of the proposed LNA.

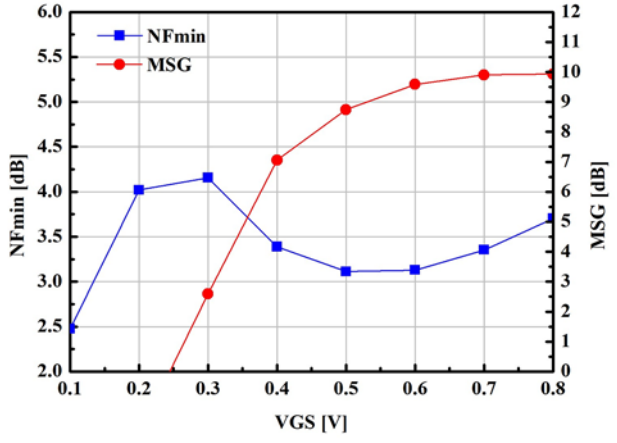

Figure 4. The simulation results of NF_{min} and MSG of a common-source topology.

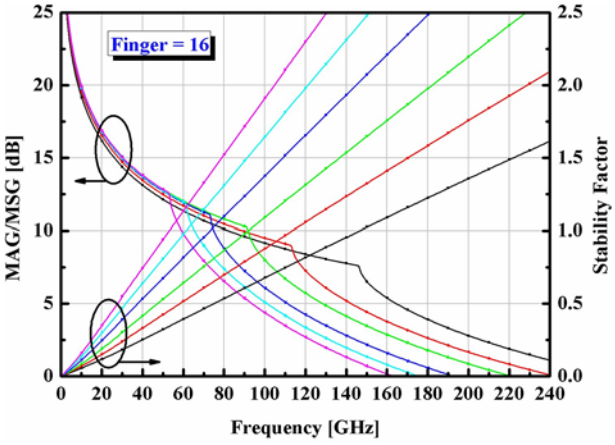

Figure 5. MSG/MAG and stability factor of common-source in different width.

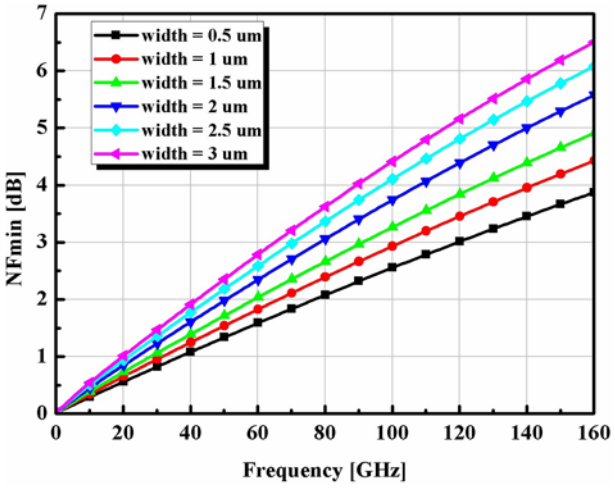

Figure 6. NF_{min} of common-source in different width.

does not degrade tremendously, while the dc power consumption can be lowered. Nevertheless, in the proposed circuit, noise performance is more important than gain performance. Therefore, a small amount of gain is traded off and the V_G bias is chosen at 0.58 V for better noise performance. Figure 4 shows the simulation results of NF_{min} and MSG of a CS topology.

For the device size selection, it can be divided into two main parts. The first is the selection of transistor size of CS topology,

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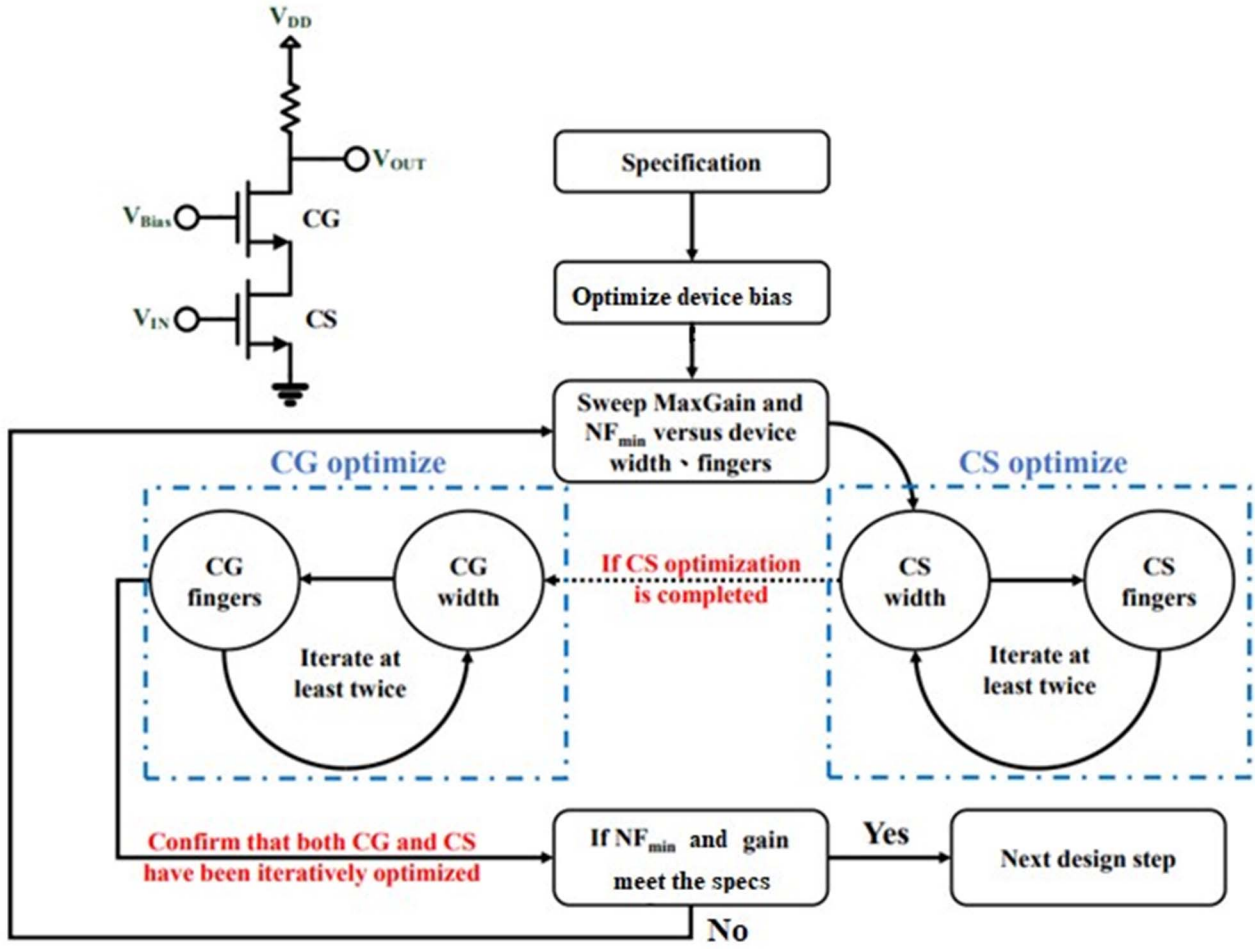

Figure 7. The design flow diagram of the cascode topology for cascode stages of LNA.

and the second is the selection of transistor sizes of cascode topology. For the first stage, MSG/MAG, NF_{min}, and stability factor are simulated for different device sizes under the same bias conditions. Figure 5 shows the MSG/MAG and stability factor of CS in different width and Fig. 6 shows NF_{min} of CS in different width. At last, the transistor size chosen for the first stage is 1.5 μm × 16 fingers. At this device size, the impedance is easier to match to 50 Ω and the NF_{min} value is kept at a good level.

Next, for the transistor sizes of cascode topology, transistors with the above selected size (1.5 μm × 16 fingers) are initially selected for both transistors. Then the size of each transistor is iterated by sweeping the width and fingers. Since CS topology is used in the first stage to reduce the noise as much as possible, if the later stages also prioritize noise before gain, the overall gain of the circuit may be insufficient. Therefore, gain is the priority in the cascode topology. In the end, the transistor sizes of the cascode topology were selected as 2 μm × 26 fingers and 2 μm × 20 fingers respectively by the process in Fig. 7. The V_G biases of cascode topology are fine-tuned to 0.58 V/1.48 V.

Matching network

While LC matching networks are effective in minimizing circuit size, it is important to note that the use of low-Q capacitors and inductors can result in higher loss and reduced efficiency compared to TL networks [13]. Hence, the decision between LC matching and TL matching necessitates striking a balance between efficiency and chip area. Figure 1 shows the overall architecture of the matching network using thin-film microstrip lines for three-stage design. Figure 1 also shows the replacement of the two TLs with inductors (L_1, L_2). To achieve a reduction in chip area without compromising efficiency significantly, it is deemed acceptable to utilize inductors in these specific sections instead of TLs. In the 28-nm CMOS HPC-plus process, the metal layers are in close proximity to the ground, leading to a strong parasitic effect. To mitigate this, the ground will be selectively removed from sensitive areas to enhance matching. Additionally, the top metal layer (M9) will be employed to implement the TL, as depicted in Fig. 8. It is worth noting that due to process limitations, we do not have access to a momcap cell. Consequently, we need to design the bypass capacitors ourselves. This is necessary in order to comply with the design rules and achieve the required capacitance. As a result, a significant amount of space is occupied to ensure sufficient capacitance. Figure 9 shows the simulation result of the designed bypass. A −20 dB insertion loss is achieved to ensure an ideal ground across the designed bandwidth. The input and interstage matching use the L-type networks, while the output matching adopts the T-type network to provide a wideband output matching. The gm-boosting and the noise reduction techniques (mentioned in the "Circuit design" section) are utilized to enhance the gain performance.

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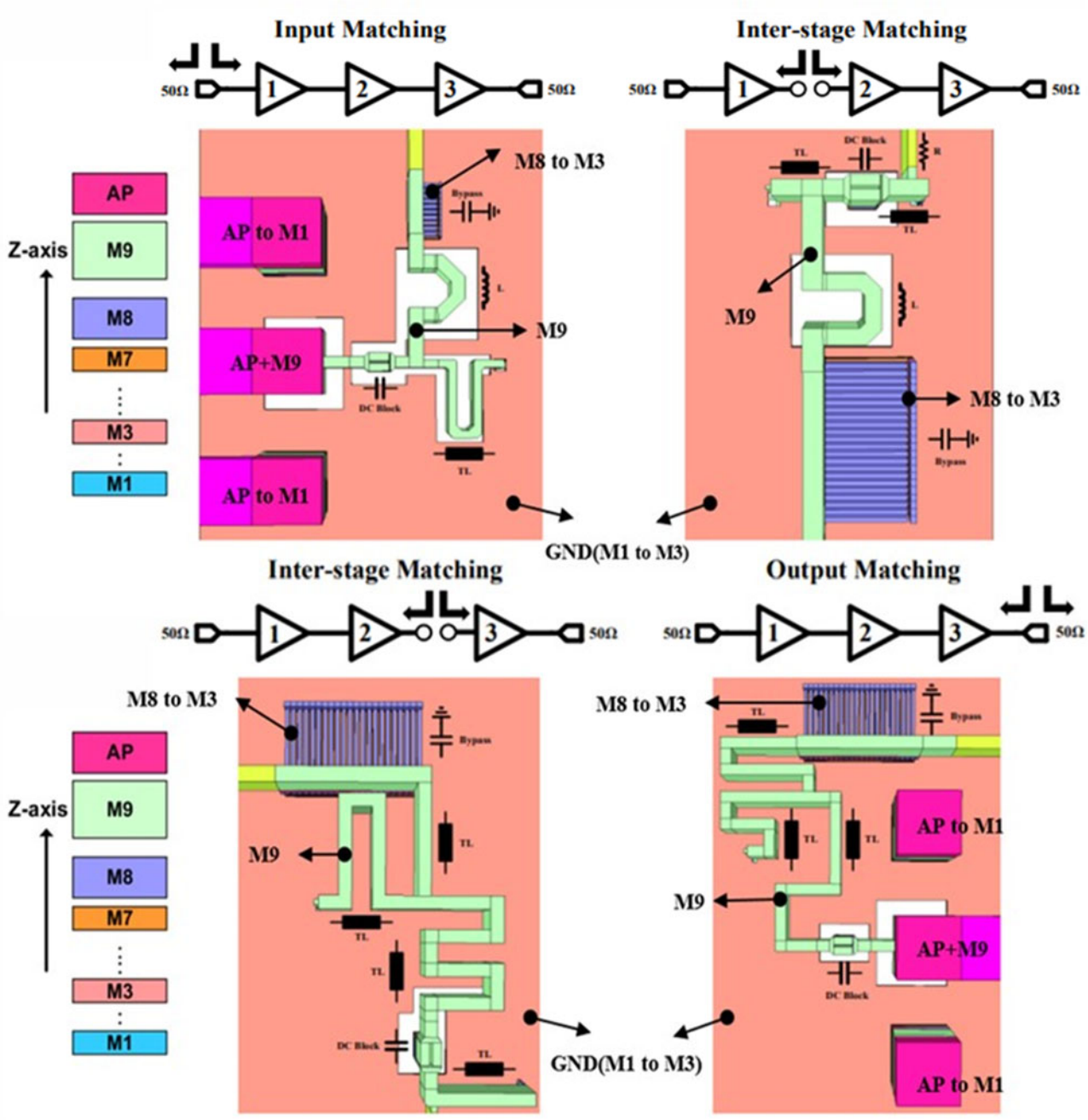

Figure 8. Matching networks of the proposed E-band LNA.

Measurement results

The proposed three-stage E-band LNA is implemented in a 28-nm CMOS HPC-plus process, utilizing Sonnet for electromagnetic (EM) simulation to calculate parasitic loss. The overall size (see Fig. 10), including all pads, is 0.695×0.715 mm^2.

The small-signal S-parameters of this LNA were measured by Keysight N5225B Performance Network Analyzer (PNA) network analyzer and Keysight N5295AX03 frequency extender with an input power of −30 dBm via on-wafer probing (see Fig. 11). Figure 12 shows the measured and simulated S-parameters. It achieves a peak gain of 16.8 dB with a gain variation of less than ±0.5 dB from 67.8 to 90.4 GHz. The 3-dB bandwidth is about 30 GHz (64–93.8 GHz). The NF of this LNA was measured using the Y-factor method with a Keysight E4440A spectrum analyzer, a Quinstar QNS noise source, a mixer to lower the frequency, and a preamplifier to improve the system noise floor. Due to the limitation of instruments, NF was measured only up to 74 GHz. The measurement setup is shown in Fig. 13. To verify the repeatability of the chips, two samples were measured and they showed similar results. The measurement results are also in agreement with simulation results, as shown in Fig. 14. The measured NF is below 5 dB from 66 to 74 GHz, and the measured minimum NF is around 3.8 dB at 73 GHz. The measured noise performance exceeds the simulation, mainly due to the overestimation of parasitic losses in the EM simulation. The large signal

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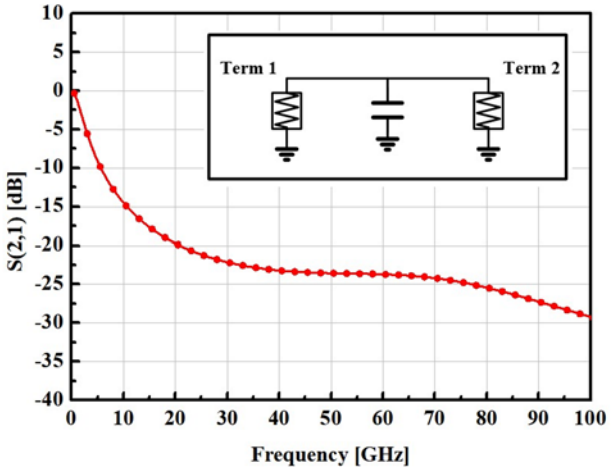

Figure 9. Insertion loss of the designed bypass.

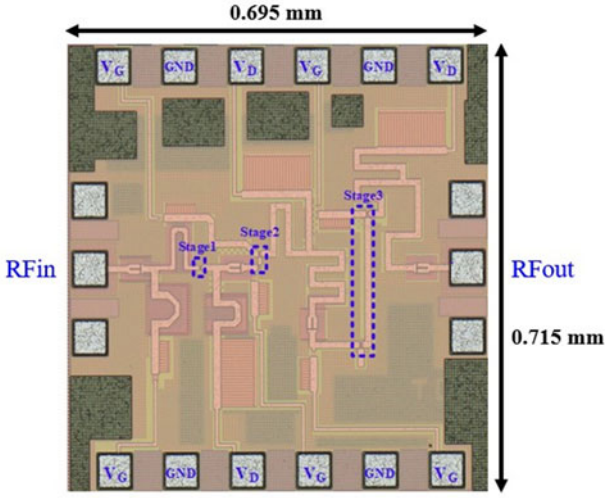

Figure 10. Chip photo of the proposed E-band LNA.

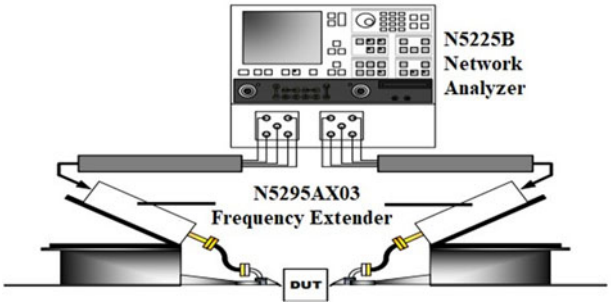

Figure 11. Small signal measurement setup.

performance of this LNA was measured by Keysight E4440A spectrum analyzer with down-conversion mixer, while the signal was generated by Keysight E8267D signal generator. The LNA achieves an IP_{1dB} of −14 dBm and an OP_{1dB} of 1 dBm at 80 GHz (near center frequency) as shown in Fig. 15. The IIP_3 is −4 dBm for the LNA, as measured by two-tone measurements and shown in Fig. 16. Table 1 summarizes the performance of published E-band LNAs in recent years. The proposed three-stage E-band LNA demonstrates excellent performance in terms of gain flatness and NF. Its NF surpasses that of III–V compound semiconductors in references [14, 15], highlighting the cost-effectiveness and superior performance of the CMOS process.

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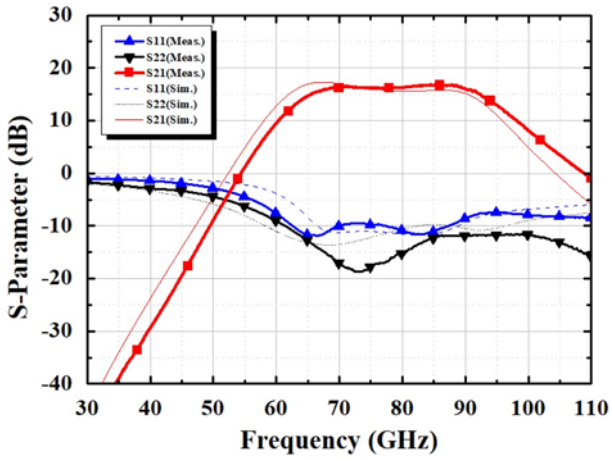

Figure 12. Measured and simulated S-parameters of the proposed E-band LNA.

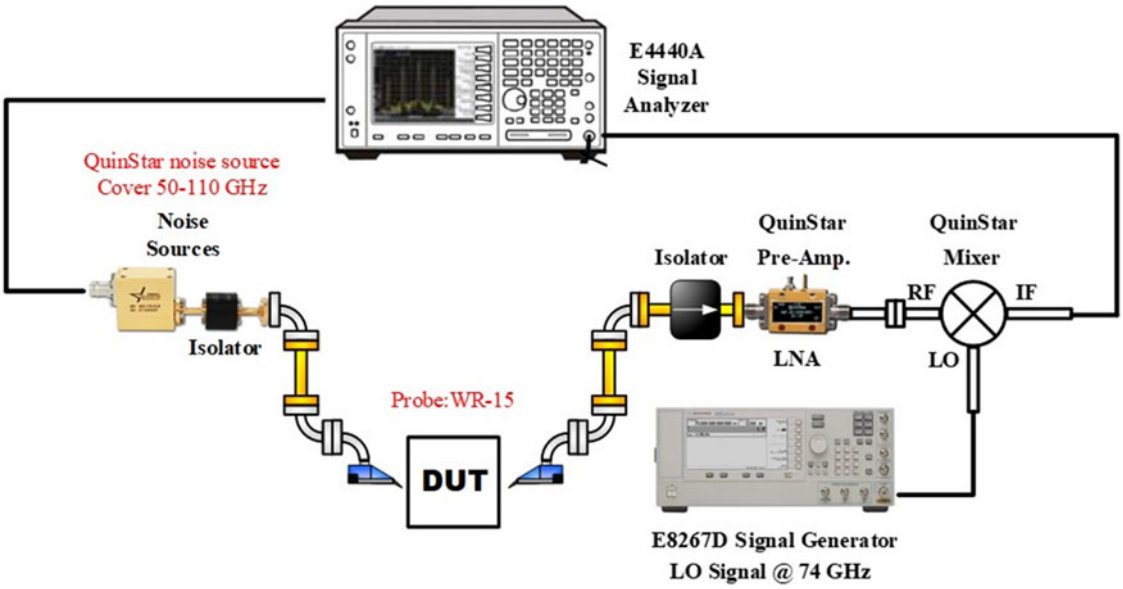

Figure 13. Noise figure measurement setup for the proposed E-band LNA.

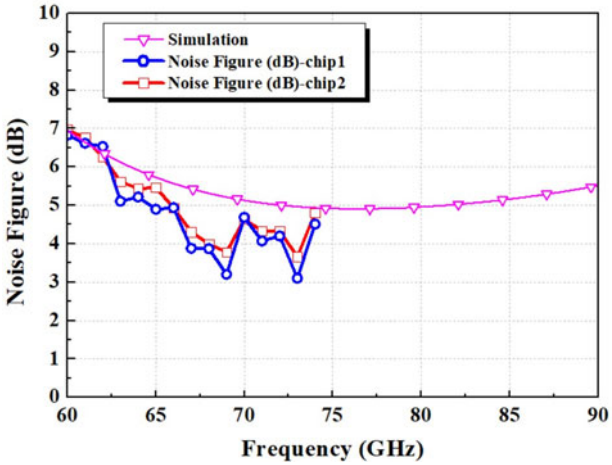

Figure 14. Measured and simulated noise figure of proposed E-band LNA.

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Table 1. Comparison of the published E-band LNAs and Variable Gain (VG)-LNAs

Reference	Technology	Topology	3-dB bandwidth (GHz)	±0.5 dB bandwidth (GHz)	Min. NF (dB)	Peak gain (dB)	IP_{1dB} (dBm)
[1] JSSC'17	65-nm CMOS	4-stage common-source	54.4–90	60–75[a]	5.4	17.7	−14
[2] EuMIC'18	90-nm CMOS	3-stage cascode + 1-stage common-source	68.8–87.6	82–86[a]	5.3	23	N/A
[3] TMTT'20	22-nm CMOS Fully Depleted Silicon On Insulator (FDSOI)	3-stage cascode	70–85[a]	75–82[a]	4.6	24	−26.8
[4] APMC'18	90-nm CMOS	1-stage common-source + 2-stage cascode	66–70	66.5–68.5[a]	8.8	20.2	N/A
[5] MWCL'19	65-nm CMOS	3-stage cascode	60–90	63–84[a]	6.3	14.2	−10
[6]RFIC'18	45-nm CMOS Radio Frequency Silicon On Insulator (RFSOI)	2-stage common-source + 1-stage cascode	74–99	80–94[a]	4.2	12	−21
[7] MWCL'21	28-nm bulk CMOS	5-stage common-source	82–91[a]	83–89[a]	6	25	−32
[8] MWCL'17	28-nm CMOS FDSOI	3-stage common-source	55–70[a]	58–65[a]	6	17	N/A
[14] MWCL'22	130-nm SiGe	2-stage common-emitter	62–110	70-92[a]	4.5	13.5	−12.5
[15] MWCL'20	100-nm GaN	3-stage common-source	77.8–84	79-81.5[a]	3.8	20.5	N/A
		3-stage common-source	78.5–90	79.8-88[a]	4.5	17	N/A
This Work	**28-nm CMOS HPC+**	**1-stage common-source + 2-stage cascode**	**64–93.8**	**67.8–90.4**	**3.8**	**16.8**	**−14**

[a]Estimated from the figure

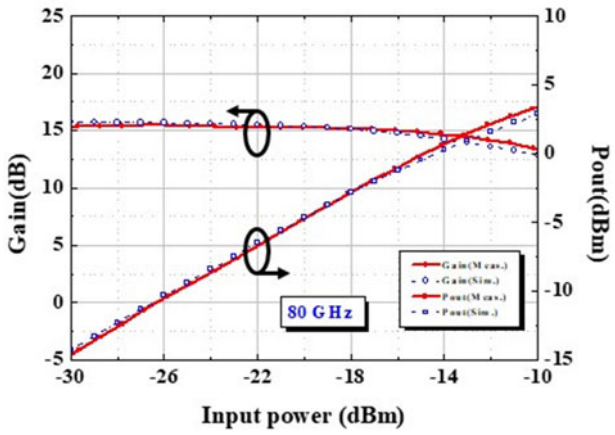

Figure 15. Measured and simulated power performance of the proposed E-band LNA at 80 GHz.

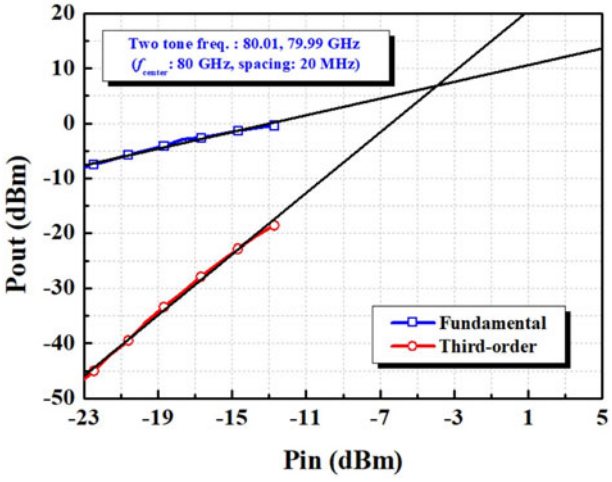

Figure 16. Two-tone measurement of the proposed E-band LNA at 80 GHz.

Conclusion

In this paper, an E-band three-stage LNA with high gain flatness and low NF fabricated in 28-nm CMOS HPC-plus process is presented. It achieves a peak gain of 16.8 dB with a gain variation of less than ±0.5 dB from 67.8 to 90.4 GHz. The 3-dB bandwidth is about 30 GHz (64–93.8 GHz). The measured NF is below 5 dB from 66 to 74 GHz, and the measured minimum NF is around 3.8 dB at 73 GHz. By utilizing one-stage common-source with two-stage cascade topology, the proposed E-band three-stage LNA achieves extremely high gain flatness and low NF compared with recently published E-band CMOS LNAs.

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Competing interest. The authors report no conflict of interest.

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