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# Strain Profiles in Si Channel of PMOS Devices Affected by Shallow-Trench Isolation Strain Relaxation In Embedded SiGe

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Shallow-trench isolation (STI) induced strain in the moat of Si has been studied extensively by using transmission electron microscopy (TEM) based techniques, such as Convergent Beam Electron Diffraction [1] and dark-field electron holography [2]. However the STI proximity effect on the strain in strained Si devices with embedded SiGe (eSiGe) Source/Drain (S/D) has not yet been analyzed. Also the shape of eSiGe S/D is critical to channel strain for advanced technology. In this report, we used Nano-Beam Diffraction (NBD) and Geometric Phase Analysis (GPA) to study the channel strain distribution effect by STI proximity, and the shape of eSiGe S/D.

The NBD technique has been optimized for scanning transmission electron microscopy (STEM) measurements of strain in fully processed devices. The experiments were performed on dedicated Hitachi HD-2300 STEM with an AMT 2k x 2k camera. Strain resolution has been determined to be 0.002, with 5 nm spatial resolution. The HAADF-STEM images for GPA analysis were carried out on an FEI Titan 80-300 TEM/STEM with a Fischione annular dark field detector. Strain resolution has been determined to be 0.002, with 3~5 nm spatial resolution.

In Figure 1a, the strain distribution as determined by NBD is shown. The larger lattice spacing in eSiGe S/D creates a compressive strain, $\varepsilon_{x[110]}$ in the channel, and a tensile strain in the S/D area. As shown in Fig.1(b), the channel strain decreases as the transistor gets closer to the STI (active edge). This is a result of eSiGe strain relaxation at the STI/SiGe interface.

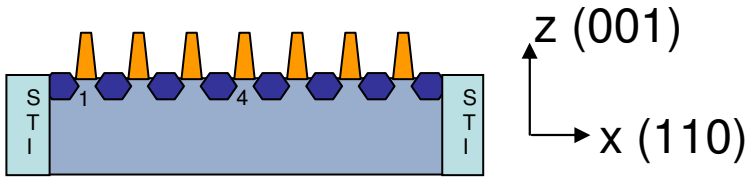
In order to determine the magnitude of the decrease in channel strain from edge to center, the average channel strain values were obtained from both GPA and NBD techniques. They are compared in Table 1 for both $\varepsilon_{x[110]}$ and $\varepsilon_{z[001]}$. Since the GPA and NBD data was taken on two different but comparable structures with slightly different thicknesses, possibly resulting in different amounts of strain relaxation, the values of $\varepsilon_{x[110]}$ do not match exactly between two techniques. However, the difference in strain in $\varepsilon_{x[110]}$ between the edge (transistor 1) and center (transistor 4) in these two techniques are comparable. GPA shows an offset of 0.003 and NBD of 0.002 strains. This indicates a significant amount of channel strain reduction, from strain relaxation at the active edge.

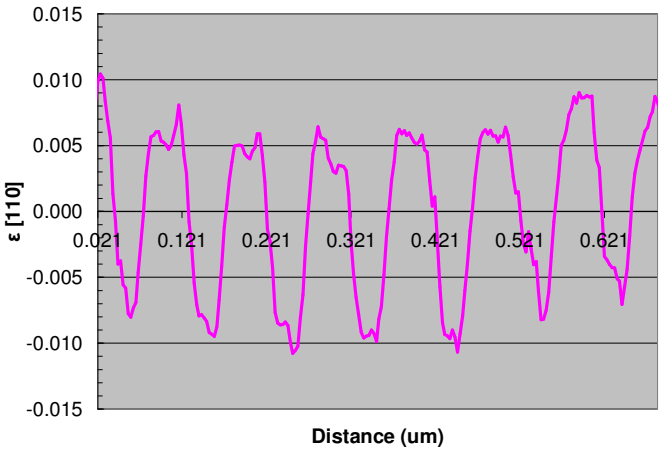
In Figure 2, the STI proximity effect on transistor drive current is shown for PMOS transistors formed in the same process, using diamond shape eSiGe, as used in the strain measurements. There is a significant saturated drive current, $ID_{SAT}$, degradation near the STI, compared transistors closer to the center. This result correlates to the channel strain measurements, confirming the trend that strain relaxation occurs near STI edges.

PMOS advanced technology with eSiGe S/D have been investigated from the perspectives of STI proximity effects. Both GPA and NBD strain measurement techniques and electrical data show that strain relaxation can result in a significant STI proximity effect in devices with diamond shape eSiGe. This effect could be a cause of transistor performance variation in future CMOS technology.

[1] Armigliato, R. Balboni, and S. Frabboni, Appl. Phys. Lett. 86, (2005) 340
[2] M. Hÿtch1, F. Hüe1,2, F. Houdellier, E. Snoeck and A. Claverie, IEDM (2009) 39

(a)




(b)

Fig 1. Image showing layout of device in cross-section (a) and corresponding horizontal $\varepsilon_{x[110]}$ strain profile by NBD (b) from an array of 7 transistors.

| | GPA | | NBD | |
|---|---|---|---|---|
| Device # | 1 | 4 | 1 | 4 |
| $\varepsilon_{x[110]}$ | -0.008 | -0.011 | -0.006 | -0.008 |
| $\varepsilon_{z[001]}$ | 0.007 | 0.008 | 0.006 | 0.007 |

Table 1. Strain comparison between edge (1) and center (4) transistors analyzed by GPA and NBD.

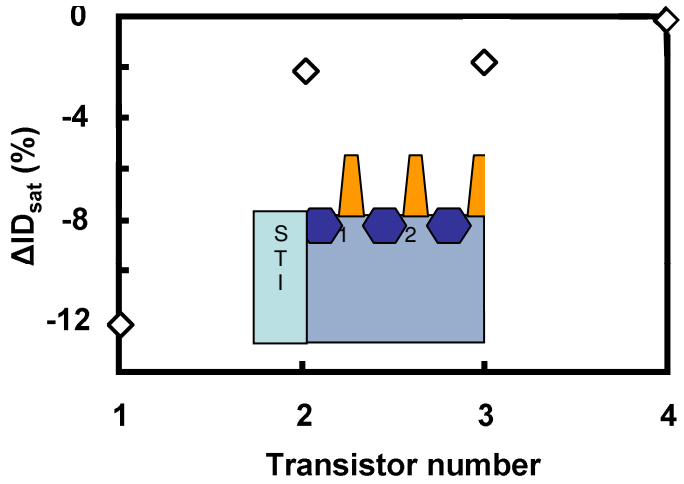



Fig 2. Comparison of change in drive current in the saturation region, $\Delta ID_{sat}$, for transistors at various distances from the STI, for diamond shape eSiGe.

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