Characterization of GaN E-mode HEMT Devices by In-Situ STEM Electrical Biasing

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The gate failure mechanism is an integral part of the p-GaN-based E-mode GaN high electron mobility transistors (HEMTs) reliability study, as the p-GaN gate cap controls the formation of 2-DEG in the channel. Thus, the robustness of the p-GaN gate majorly dictates the performance and operation of the device. Literature survey shows the gate failure mechanism to be operating condition dependent; like time-dependent dielectric breakdown (TDDB) [1], it also depends on factors like the acceptor doping concentration [2], operating voltage and temperature [3-5], physical design and dimensions of device [2,4]. Because of these varying and operation-dependent breakdown mechanisms, it becomes necessary to identify electrical and physical signatures associated with gate failure. To our knowledge, no prior work has been done on in-situ biasing of a single GaN-based HEMT device in TEM/STEM. We aim to study gate breakdown in real-time while simultaneously applying a bias to the gate.

This work describes the sample preparation and in-situ biasing of the E-mode p-GaN based GaN HEMT device. A single gate-source structure is studied in real-time using novel sample design and fabrication from commercially available E-mode GaN HEMT devices using Focused Ion Beam (FIB). The fabricated sample is subjected to a forward bias sweep to record the gate characteristic and changes during the bias. External SMU was used to apply forward bias and capture current data. Figure 1 shows the electrical circuit used for the particular in-situ biasing experiment. The current value shown in figure 2 helps us verify the proper electrical circuit even after lifting one device out of the chip. Scanning Transmission Electron Microscopy (STEM) imaging shown in figure 3 suggests the electrical stress generated due to biasing results in a physical change in the device.

Our results show the E field developed due to biasing results in mechanical stress responsible for strain in the sample. This results in physical deformation confirmed by dislocation contrast. We also see Ga diffusion under the influence of a high E field during forward bias. Ga diffusion can lead to charge leakage paths and increased current leakage from the gate. We further suspect that the Ga diffusion makes the GaN lose its intrinsic property to withstand high E-field, and thus low voltages can result in device degradation. Nano-micro level changes due to biasing help us identify key factors affecting device reliability during its continuous operation. Furthermore, we noticed that the p-GaN/AlGaN and AlGaN/GaN interface shows localized discontinuity with the presence of interlayer diffusion in the heterostructure.

This study helps us to visualize the electric field's effect inducing physical changes at the p-GaN layer and AlGaN interface on the p-GaN and GaN sides. With a focus on the real-time changes occurring in the gate region of the device, gate breakdown failure and its mechanism can be well understood [6].
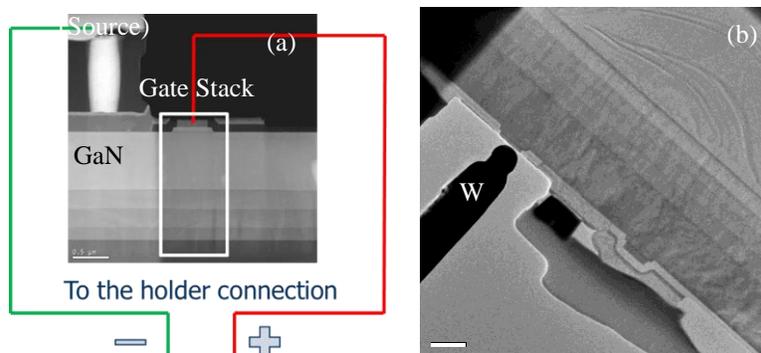
Figure 1. (a) Schematic representation of Gate/source sample with electrical circuit imposed sample design and (b) TEM image showing sample assembly inside TEM before biasing.
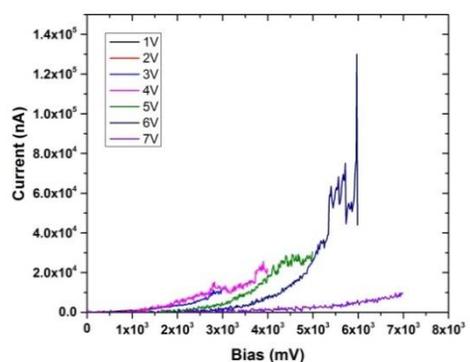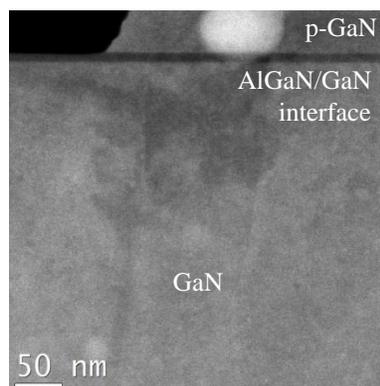

Figure 2. Electrical Biasing I-V data.

Figure 3. STEM HAADF image showing Ga globule, dislocation contrast in the p-Gan region.

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