International Journal of Microwave and Wireless Technologies

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A novel frequency down-converter design at X-band for LEO satellite ground station using single conversion

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Research Paper

Cite this article: Sisman I, Ergin TH, Barkana DE (2024) A novel frequency down-converter design at X-band for LEO satellite ground station using single conversion. *International Journal of Microwave and Wireless Technologies*, 1–11. https://doi.org/10.1017/S1759078724001156

Keywords:
down-converter; LEO; satellite; single conversion; X-band

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Abstract

This paper presents the design and implementation of a broadband down-converter system using the AWR (Advancing the Wireless Revolution) modeling and Microwave Office tool. The radio frequency (RF) signal coming to the antenna interface requires a frequency down-converter to be lowered to the intermediate frequency (IF) band. It includes mixing blocks, oscillators, amplifiers, step attenuators, isolators, and filters. The input frequency band (RF) is 8250 ± 250 MHz, while the output frequency (IF) band is 720 ± 200 MHz. The gain dynamic range of the circuit is expanded through the use of digital attenuators. It is a superheterodyne down-conversion circuit, combining the IF band to produce the desired RF spectrum in one pass. Two phase-locked oscillators are used at the local oscillator port of the mixer, one providing a single frequency, while the other has a programmable frequency synthesizer with 1 MHz steps in the frequency range from 7280 to 7780 MHz.

Introduction

Satellites play a crucial role in global telecommunication systems, facilitating the transmission of significant multimedia traffic. Communication satellites have been a cornerstone of the worldwide communication network for approximately 60 years. In satellite communication, the essential resources are orbits and radio frequency (RF) spectrum, with orbit being the path a satellite follows in space and frequency allocations determined by international agreements and under the management of international organizations [1–4].

There are several types of orbits that are designed for particular applications. In general, satellites follow an elliptical orbit with a determined eccentricity on the orbital plane defined by space orbital parameters [5–7]. The orbital eccentricity of an astronomical object is a dimensionless parameter that determines the amount by which its orbit around another body deviates from a perfect circle. In eccentricity, 0 is a circular orbit, values between 0 and 1 form an elliptic orbit, 1 is a parabolic escape orbit (or capture orbit), and greater than 1 is a hyperbola. Satellites' circular orbits are classified as geosynchronous Earth orbits, medium Earth orbits, and low Earth orbits (LEOs). The main difference is in the altitude above the Earth's surface, which further impacts the satellite's velocity and the orbital period in the appropriate orbit [8–10]. LEO is typically between 300 km and 1400 km above Earth's surface. The lower altitude range is limited by the Earth's atmosphere, where almost no air exists, preventing the satellite's speed reduction and drag down necessary for it to remain in orbit. The inner Van Allen belt limits the higher altitude range, a space radiation zone with undesirable effects on a satellite's payload and platform, making it unsuitable for LEO satellite accommodation [10]. LEO satellites travel at a velocity of approximately 7.2–7.5 km/s relative to a fixed point on Earth (a ground station). It takes them around 90–110 minutes to complete one orbit around the Earth. The time for communication between a satellite and a ground station varies depending on the orbital altitude, occurring 6–8 times a day and lasting between 5 and 15 minutes. LEOs are unique because they have the shortest distance from Earth than other orbits, resulting in minimal time delays [8–11]. These properties make LEOs particularly remarkable for communication and other applications.

Up- and down-converters translate intermediate frequency (IF), typically 70–140 MHz, and the actual uplink and downlink frequencies, respectively. The output power level from the down-converter should be sufficient to stimulate a demodulator. The output power level from the up-converter should be adequate to drive the power amplifier [12, 13].

A typical down-converter amplifies the signal to provide a sufficient gain for the operation of the station equipment. The down-converter is positioned behind the low noise amplifier (LNA) and it is estimated that there will be elements such as filters, amplifiers, mixers, oscillators, frequency synthesizers, couplers, etc. They operate at high frequencies and their characteristics

vary according to frequency, bandwidth, and high-frequency output power. The parameters of these elements are highly dependent on each other [14]. After the LNA, down-scaling the RF signal to the IF band level is desired. Because the user needs a frequency down-converter sub-system in terms of cost-effectiveness, and elimination of interference, which is one of the disadvantages of high frequency, and because the modem input signals are IF band. This unit is expected to down-converter the received RF signal in the 8–8.5 GHz frequency band to 720 MHz frequency with $\pm$200 MHz bandwidth. Since the output of this subsystem will be used by the modem, image rejection, phase noise, noise figure, and local oscillator (LO) leakage values should be low.

The frequency converter system includes a frequency-lowering RF module, control circuit board, and power supply, each in its mechanical box. The device box to be developed will be suitable for use in satellite systems. The requirements that frequency converters should meet are spurious levels, gain ripples, Voltage Stating Wave Ratio (VSWR), noise figure, output signal power level, and signal linearity. The essential working concept for these requirements can be listed as hairpin filter, coupler, RF block diagram (X-band and IF band), frequency synthesizer, regulator circuit, control card, and mechanical design.

The X-band circuit design, which covers the processes in which the incoming signal is obtained until it is delivered to the RF input of the mixer, is designed and realized with the help of modeling of the specified materials and equipment. The IF band circuit design, which covers the operations until the signal received from the IF output of the mixer is delivered to the frequency converter output, is designed with the help of modeling of the specified materials and equipment. The phase-locked loop (PLL) is a block created to generate the LO signal required for frequency conversion in a more stable way [22]. The PLL divides the frequency of the signal produced by the voltage-controlled oscillator (VCO).

PLL compares the phases of the signal produced by the reference oscillator and enables the VCO to produce a signal at the desired frequency. The stable reference signal produced by the reference oscillator is the input signal of the PLL block [23, 24]. The frequency stability of the reference oscillator varies with time and temperature. A microcontroller control circuit is designed to control the frequency converter system's gain, level compensation, and alarm conditions. The control circuit includes RS232 serial communication and ethernet communication units that can be connected to the panel output of the product.

Dual conversion and single conversion are used to lower the broadband frequency in the limited amount of studies available in the literature as seen in Table 2. It is not very commonly found in the literature because it affects the performance of the solution with a single stage mixer in this wide band. However, in the contribution of our study, we do this in a novel and successful way in very broadband with a single conversion. Ensuring frequency stability is crucial for maintaining the integrity of the down-converted signal. Even slight frequency shifts can lead to significant performance degradation in X-band systems. High-stability components such as stable oscillators and low phase noise mixers were selected for this system, and thermal pads were used to minimize frequency variations through temperature balancing. Consequently, a phase noise value of −74 dBc/Hz@100 Hz was measured. High phase noise can significantly degrade the quality of down-converted signals, especially in high-frequency communication systems like X-band. Minimizing phase noise involved careful selection of low-noise components and shielding the frequency synthesizer unit by designing it as a separate circuit board from the main circuit. This approach positively impacted the phase noise performance. Maintaining linearity and sufficient dynamic range within the system, particularly challenging due to the presence of strong parasitic and multi-tone signals, was crucial. In achieving this, it was important to maintain stability within the working frequency range without amplifying signals in the RF stage and keeping unwanted frequencies at low levels within the transition band. Additionally, coplanar waveguide technology was employed for the high-frequency lines carrying signals in the frequency synthesizer unit, ensuring good planarity, high-frequency performance, low loss, and smooth impedance matching, thereby reducing phase noise and spurious values from the frequency synthesizer. In the IF section, high rejection filters and low-distortion amplifiers were preferred to enhance the overall performance of the design. As a result, the system achieved +13.86 dBm output P1dB, −63 dBc spurious level, −88 dBm LO leakage, and 70 dB image rejection. Single-stage mixer architecture was utilized to provide wide dynamic range, effectively mitigating intermodulation distortions. Achieving −88 dBm LO leakage, −63 dBc spurious level, and 70 dB image reject in such a wide dynamic range with a single-stage mixer structure is challenging. However, we successfully achieved high performance in a wide dynamic range with a single-stage mixer structure in our design. In this study, the best performance in the frequency down-converter is achieved using a single LO mixer stage. Compared to the literature, providing such high performance at close LO and RF frequencies in terms of frequency is challenging, and we have achieved this challenge in our design.

Design specifications

The frequency down-converter is used in the terminals of satellite communication systems and ground stations, which can be fixed cabins and moving platforms [25].

The frequency converter unit is used after the antenna of the ground station and the LNA unit to down-convert the RF signal received from the satellite to the IF frequency and transmit it to the modem [26]. The important part of the design of the frequency down-converter is generating filter, coupler, RF block diagram (X-band and IF band), frequency synthesizer, regulator circuit, control card, and mechanical design. In addition to this, the requirements that frequency converters should meet are spurious level, noise figure, image rejection, phase noise, output P1dB, and LO Leakage. X-band frequency down-converter specifications are seen in Table 1.

The LO signal is generated by a VCO. A feedback loop and PLL control the voltage control. This loop compares the phase of the VCO and the crystal oscillator and generates a square wave at kHz or MHz frequencies. This square wave is filtered with a low-pass filter and converted into a DC signal. VCO frequency is controlled with this DC signal. In a PLL, it is desirable to have low levels of phase noise and spurious signals at the end of the loop.

Image frequency is the frequency that, after mixing produces the same IF signal as the fundamental RF signal. In receivers, the correct filters must be used to suppress this frequency. Spuriouses are signals consisting of the product of the input signal and the fundamental or higher harmonics of the LO signal. Correct filter selection provides these signals suppressed in the output spectrum.

The control circuit in the system provides control of the gain level by changing the states of the RF digital attenuator. An important parameter is the image rejection level of the frequency down-converter to be used at the receiver side of the satellite communication system. This parameter is related to the characteristics of the

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Table 1. Specifications of the X-band frequency down-converter

Parameter	Value
Input operating frequency	8–8.5 GHz
Output operating frequency	0.72 GHz (±200 MHz)
1 dB compression point	+13 dBm
Gain adjustment step	1 dB
Input reflection ratio	15 dB
Output reflection ratio	15 dB
Local oscillator frequency	7.28–7.78 GHz
Local oscillator leakage	−70 dBc
Image frequency rejection ratio	−70 dB
External reference oscillator frequency	10 MHz
External reference oscillator signal level	−5 ⋯ +5 dBm
Noise factor	Max 20 dB
Phase noise	−64 dBc/Hz (@100 Hz)
Voltage	220 V AC
Input connector type	N
Output connector type	N

filter to be used at the input. According to the input and output frequencies, the frequency band of the image frequency is calculated, and the filter is selected accordingly. The phase noise is another determining parameter for the frequency down-converter. The low phase noise of the design is critical in satellite communication links where phase modulation is generally used. The level of spurious signals is also an essential parameter for the cleanliness of the signal band.

Various previously developed commercial frequency down-converters features have also been provided in Table 2. For these commercial products, the bandwidth, image rejection value, spurious level, phase noise, LO leakage level, and noise value outside the operating frequency band are very important in terms of performance determination.

The difference between our design and similar ones in both commercial and literature contexts lies in the fact that while we use a single conversion structure to convert a wide X-band RF signal to an IF signal at 720 MHz, the comparable designs typically employ a dual conversion structure. This showed that a product with this feature can perform better than its other counterparts. It is very difficult to achieve such high performance with superheterodyne designs. The new design we offer has reduced the design's complexity and provided higher performance compared to other products in this regard. In the performance comparison of commercially available products, 1st product [15] gives the best performance outputs compared to products [16], [17], [18]. However, compared to the product [15] of the new design we presented, our image rejection value, output P1dB value, phase noise, spurious level, and noise figure value gave better performance output. These excellent performance outputs prevent the formation of unwanted harmonics in the carrier signal when decoding the broadcast from the satellite in modems, which are the latest terminal units in ground station systems. This is an important requirement in ground station systems. In addition to this upon reviewing the studies referenced in the literature, [19], [20], and [21], it is noted that the phase noise values are provided at 1 MHz for the PLL circuit within the system. This indicates that the phase noise value offered by the presented study is significantly better.

Various subcircuits

The block diagram of the X-band frequency down-converter is given in Figure 1. The table of components for block diagram is seen in Table 3. The simulations were done in the AWR (Advancing the Wireless Revolution) simulation program. The RF and PLL parts are presented as separate design diagrams in the design. The PLL design was also performed in the AWR simulation program. The procedure is done like this because it observes the effect of the spurious level coming from PLL. This section will explain the filter, coupler, RF/IF blocks, frequency synthesizer, regulator, control card, and mechanical box subsections we have designed separately.

Filters

These filters are "Hairpin" filters operating in the frequency range of 8–8.5 GHz, and their design is shown in Figure 2(a). The specifications of hairpin bandpass filter is seen in Table 4. The characteristics of center frequency, bandwidth, insertion loss, return loss, and filter type are defined. Rogers substrate material used in high frequency applications was selected for the design. The dimensions of the hairpin resonators were calculated according to the desired center frequency and bandwidth. AWR Microwave Office simulation program was used to help us at this stage. Hairpin resonators typically consist of a quarter-wavelength resonator with one or more breaks. The number of coupling elements between the hairpin resonators was determined to obtain the desired coupling coefficient and bandwidth. The aim is to keep the image rejection value at the value in the target specification. The mixer generates image frequencies. While an RF signal source drives the mixer, and the oscillator signal from the LO port and the harmonics obtained at the output port are observed. When a mixer is used for frequency down-conversion, the input and output ports are RF and IF, respectively.

Filter simulation results as seen in Figure 2(b). Image rejection and noise figure are affected by the performance of the integrated circuits in the system diagram. A reflectionless filter is used after the mixer in the image reject mixer. The RF signal frequency is successfully passed through a hairpin bandpass filter. This prevents the generation of image frequencies in the RF stage. Improvement has been made in the system's RF stage filters and PLL stage VCO to mitigate phase noise and spurious signals in the single mixer topology.

Coupler

In the X-band frequency down-converter system design, the coupler used at the input in the RF block diagram in Figure 1 is not integrated. The specifications of coupler is seen in Table 5. A directional coupler is used in the RF stage. Basically, a directional coupler transmits a signal from one direction to another while reflecting or losing part of the signal in the other direction. These couplers usually attenuate the signal in a particular direction while transmitting a large portion of the signal in the other direction. The coupler used in the RF stage was used to measure the signal strength by sampling. The designed directional coupler has four ports: input port, transmitted port, coupled port, and isolated port. The 10 dB directional coupler design in the 8–8.5 GHz

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Table 2. Comparison between the commercial frequency down-converters and the proposed frequency down-converter

Ref	Architecture	Input RF frequency (GHz)	Output IF frequency (MHz)	Output IF BW (MHz)	Image rejection (dB)	P1dB (dBm)	Spurious level (0 dBm output) (dBc)	Phase noise (dBc/Hz)	LO Leakage (RF input) (dBm)	Noise figure (dB)
[15]	Dual conversion	7.7–8.5	720	±200	65	+10	−60	−72@100 Hz	−90	10
[16]	Dual conversion	8–8.5	720	±20	50	+10	−50	−70@100 Hz	N.A.	15
[17]	Dual conversion	8–8.5	720	±200	50	+10	−55	−70@100 Hz	N.A.	17
[18]	Dual conversion	8–8.5	720	±200	60	N.A.	−60	N.A.	N.A.	10
[19]	Single conversion	8.2–8.25	N.A.	±250	N.A.	N.A.	N.A.	−98.85@1 MHz	N.A.	N.A.
[20]	Dual conversion	8–9	N.A.	±50	N.A.	N.A.	N.A.	−114@1 MHz	N.A.	N.A.
[21]	Dual conversion	9.7–12.3	700	±250	N.A.	N.A.	N.A.	−96.25@1 MHz	N.A.	9
This work	**Single conversion**	**8–8.5**	**720**	**±200**	**70**	**+13.86**	**−63**	**−74@100 Hz**	**−88**	**9**

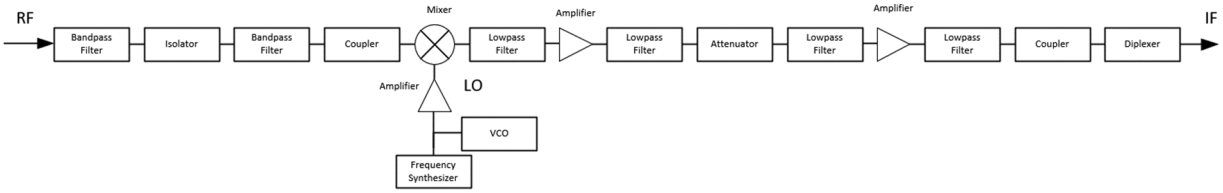

Figure 1. RF block diagram of the proposed X-band frequency down-converter.

Table 3. The table of components for block diagram

Block name	Components
RF	Hairpin filter, isolator, coupler
IF	Filter, amplifier, digital attenuator, coupler, diplexer
LO	Amplifier, VCO, frequency synthesizer

range is shown in Figure 3(a). Thanks to the couplers used at the input and output, input and output sampling data are received and processed. Figure 3(b) shows the results of the designed coupler.

RF block diagram (IF band and X-band)

The block diagram of the X-band frequency down-converter is given in Figure 1. The simulations were done in AWR simulation program using the products shown in Table 6. The RF and PLL parts are presented as separate design diagrams in the design. The procedure is done like this because it observes the effect of the spurious level coming from PLL. The three-dimensional layout of the RF design circuit is shown in Figure 4.

In the design of the X-band frequency down-converter system, band pass filter, isolator, and band pass filter were used at the input of the RF block diagram given in Figure 1. These filters are not integrated filters but designed within Profen. These filters are "Hairpin" filters operating in the frequency range of 8–8.5 GHz, and their design is shown in Figure 2(a). The aim is to keep the image rejection value at the value in the target specification. The mixer generates image frequencies. While an RF signal source drives the mixer, the oscillator signal from the LO port and the harmonics obtained at the output port are observed. When a mixer is used for frequency down-conversion, the input and output ports are RF and IF, respectively.

The design simulations were obtained by making integrated connections with input and output matching circuits. At the input

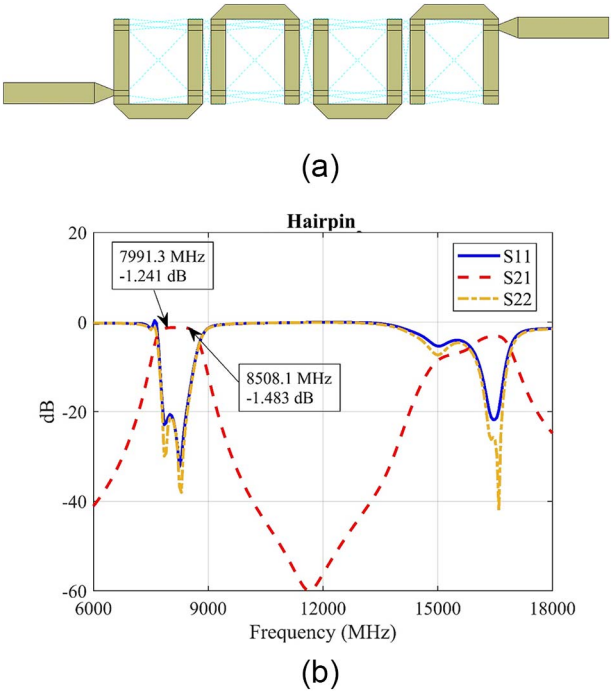

Figure 2. (a) The proposed bandpass filter (Hairpin) and (b) simulation result of the proposed bandpass filter.

of the circuit, the hairpin bandpass filter shown in Figure 2(a) is used, followed by an isolator operating at X-band frequency and again a hairpin filter with the same characteristics as the bandpass filter at the input.

The aim here is to suppress the image frequencies. Image frequencies fall in the 6.56–7.06 GHz range in the X-band frequency down-converter system. A cascade design was applied to suppress

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Table 4. Hairpin bandpass filter design specifications

Specifications	Value	Units
Center frequency	8250	MHz
Upper cut-off frequency	8500	MHz
Lower cut-off frequency	8000	MHz
Bandwidth	500	MHz
Passband ripple	0.1	dB
Return loss	−20	dB
Insertion loss	1.24	dB

Table 5. Coupler design specifications

Specifications	Value	Units
Frequency range	8000–8500	MHz
Bandwidth	500	MHz
Impedance	50	Ohm
Coupling	10 ± 0.15	dB
Insertion loss	0.25	dB
Main line VSWR	1.2	dB

this frequency range in the filter design. After the bandpass filter, the signal passes through a directional coupler and reaches the mixer. The signal level at the input of the mixer should be less than 10 dB than the LO signal.

The expected signal level at the LO input of the mixer is +7 dBm. Therefore, the IF input of the mixer should be at most −7 dBm. The mixer receives a 7 dBm signal from the PLL part. The LO power value of the selected mixer is +14 dBm. A buffer amplifier was used in the LO section to operate the mixer. The desired LO power is provided for the mixer with the amplifier used.

A reflectionless low-pass filter suppresses the harmonic and spurious signals generated after the mixer. After the filtering process, the signal is amplified with the MNA-2W [27]. After the amplification process, a low-pass filter suppresses the harmonics. MACOM AT-106-PIN [28] is a 6-bit digital attenuator. A microcontroller unit manages it. The digital attenuator provides a range of ±20 dB with its 6-bit and the criterion of being adjustable in 1 dB steps.

After the digital attenuator, the RF signal is passed through a low pass filter and then amplified with the PHA-101 [29]. The RF signal is fed to the directional coupler, where a 720 MHz center frequency signal is generated at the upper-frequency output of the diplexer. At the lower frequency output, 10 MHz external signal output is received. About 10 MHz external signal output is used for VCO. An N-type connector was used at the input and output ports, and the impedance value is 50 Ω.

Frequency synthesizer

As shown in Figure 5, the PLL circuit mainly consists of a phase sensor, load pump, filter, VCO, and N-divider. With the developing integrated circuit technologies, phase sensors, frequency dividers,

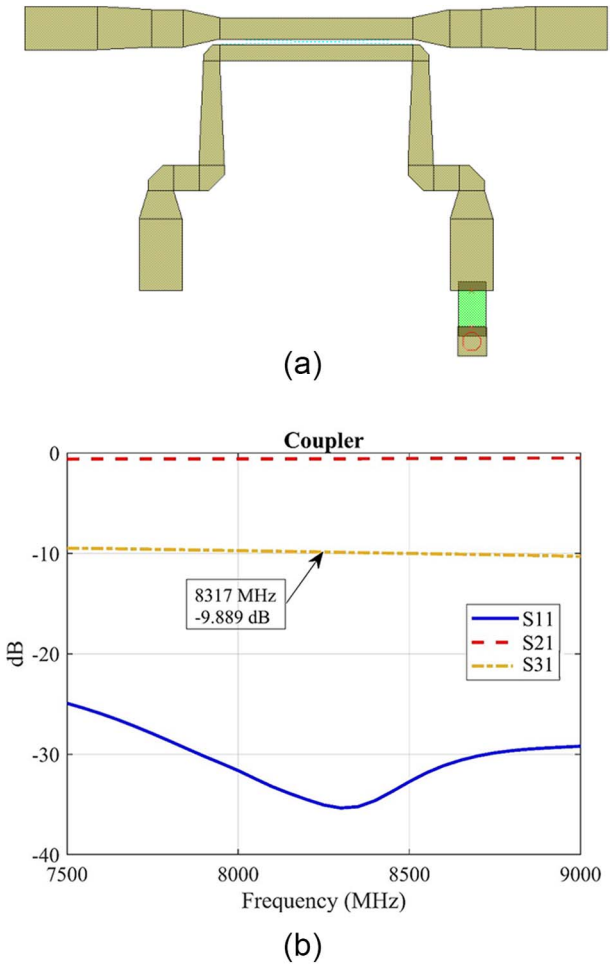

Figure 3. (a) The proposed directional coupler and (b) simulation results of the proposed directional coupler

Table 6. Integrated circuits used in the proposed circuit

Manufacturer	Product part number	Product detail
Analog devices	HMC508LP5 [30]	VCO
Analog devices	HMC703LP4E [31]	PLL
Analog devices	HMC860LP3E [32]	Voltage regulator
Analog devices	HMC976LP3E [33]	Voltage regulator
IQD	CFPT-9301 [34]	TCXO

and load pumps can be designed as integrated on the PLL synthesizer IC. As a result, in addition to dimensional gain, phase noise performance has also been improved. These combiners (synthesizers) are divided into two categories as integer and fractional. The specifications of fractional synthesizer electrical are seen in Table 7.

In integer combiners, the N value shown in Figure 5 can be integer numbers such as 200 and 201. In fractional combinators, these values can be 200.4 and 205.3. Both types of combiners have profits and losses on each other. Fractional combiners can achieve higher phase sensor frequencies for a given output frequency,

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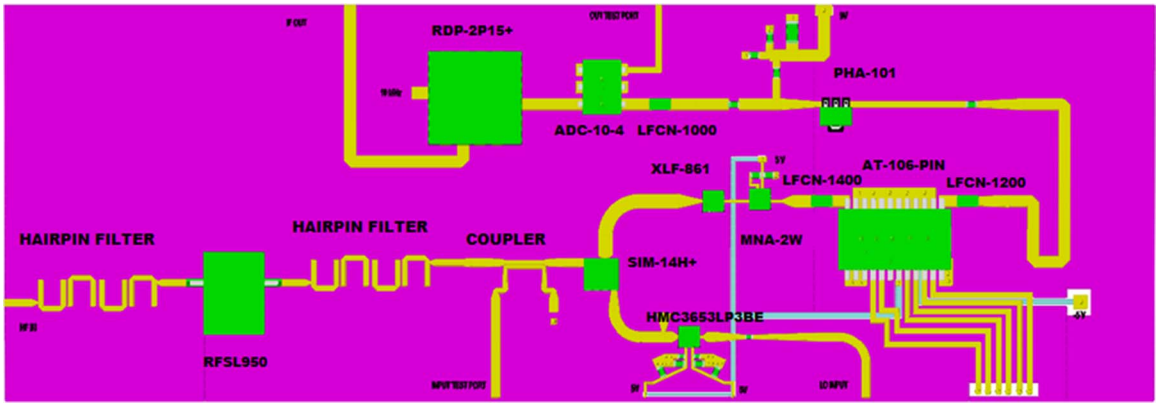

Figure 4. The proposed X-band frequency down-converter layout (21.6 cm × 10.3 cm).

which leads to a reduction in phase noise and improves the signal quality. However, at the same time, they generate unwanted signals (spuriouses) at considerably higher levels than integer combiners, which is one of the most severe drawbacks of fractional combiners. Spuriouses can be caused by the structure of the combiner or by specific external activities. The isolation of power supplies on the board, the isolation of the VCO from the digital switching circuits of the combiner, the isolation of the load of the VCO from the combiner, the isolation of the external environment, etc., are directly related to the spurious performance.

After the design requirements were determined, the combiner selection was carried out. A foreign design combiner integrated circuit chip with the best performance parameters in the market, which has a wide band frequency range of DC-8 GHz, incorporating both combiner options, has been decided. Low power signal output can be obtained at half and quarter frequencies of the output frequency.

Two types of topologies are proposed for the loop filter between the output of the combiner (load pump) and the VCO. These are passive and active filters. Passive filters can be used when the load pump can directly control external VCOs. The load pump output of the combiner used can be set between +1 and +4 V to drive VCOs. It is necessary to design an active filter with operational amplifiers for VCOs that require a higher voltage adjustment range. The effect of the active filter on the circuit should be calculated at the design point and optimized if necessary. The requirements can be met by selecting many different active filter design formats. Again, the structure in Figure 5 was analyzed with the help of the PLL circuit design program written by the company for which the combiner was designed.

The value of −64 dBc/Hz at 100 Hz is expected to be obtained in the project output. However, it is measured as −74 dBc/Hz of the currently designed circuit. This value is better than the value targeted in the project output. The three-dimensional version of the PLL circuit board planned to be fabricated is given in Figure 6. The board design given in Figure 6 is made in four stages. The reference oscillator design is also on this board. The design was made on the AWR program. Coplanar waveguide technology is used in the high-frequency lines of the design. Since the high-frequency terminals of the chips used in the design are matched to 50 Ω, no matching circuit was designed. On some lines, especially on the feedback lines, there are attenuator designs for the desired power values of the chip leads. Decoupling capacitors were used when it is necessary. The regulator circuits required for the chips are also placed on the board. Burried via circuits are used on the board, providing passing options between interstage layers.

Table 7. Fractional synthesizer electrical specifications

Specifications	Min	Max	Units
RF input frequency range	DC	8000	MHz
RF input power range	−15	−3	dBm
RF input return loss	−18	−7	dB
Phase detector rate integer mode	DC	115	MHz
Phase detector fractional mode B	DC	100	MHz
Phase detector fractional mode A	DC	80	MHz
Phase noise flicker figure of merit	−270		dBc/Hz
Spurious@8 GHz	−60		dBc

Regulator circuits

The regulator circuit converts the 220 V AC power signal from the input to 24 V DC value with the LRS-100-24 [35] coded power supply of the Mean Well. With the regulator card used in the system, a 24 V DC voltage value is used for the frequency down-converter. The 24 V DC output from here is connected to the linear LDO (low-dropout regulator). The 24 V coming to the LDO circuit is converted into 5 V, 5.5 V, 15 V, 9 V, −5 V, 12 V, 3.3 V, and −2 V and supplies other circuits. Figure 7 shows the 24 V input of the circuit and the DC voltage outputs.

Control card

In the overall block diagram given in Figure 1, the interface was added after the entire layout was formed. Because both the input frequency is variable and the gain level is desired to be adjustable, controlling it with an ethernet interface in the ground station system is necessary. Therefore, the interface design is made for the device. In the software design of the frequency down-converter, the control work of the frequency down-converter will be done with Nucleo-F429ZI [36].

X-band frequency down-converter ptcircuit tasks: (i) adjusting the attenuation amounts of the RF digital attenuator, (ii) measuring the power level with the analog output of the RF log power

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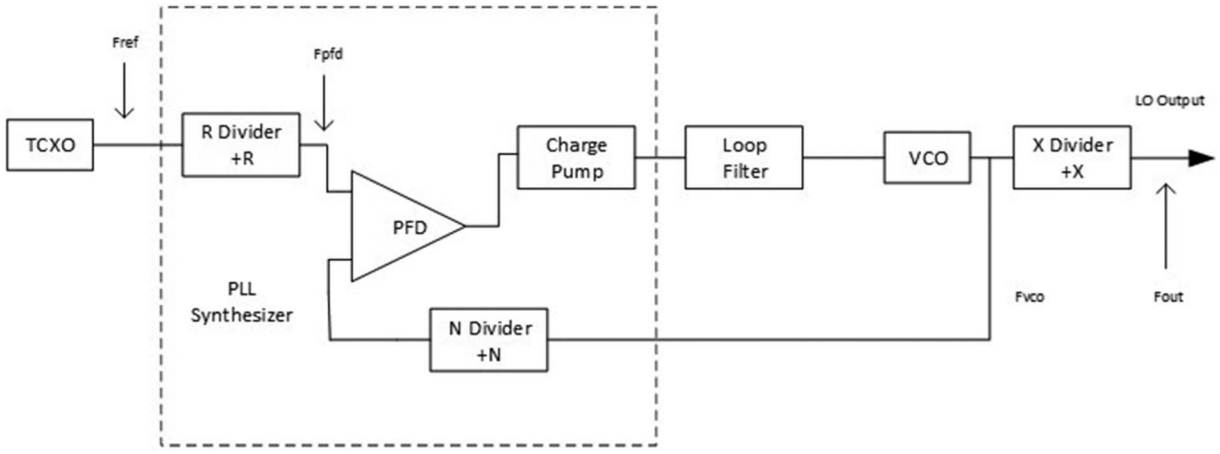

Figure 5. The block diagram of the proposed a phase-locked loop circuit.

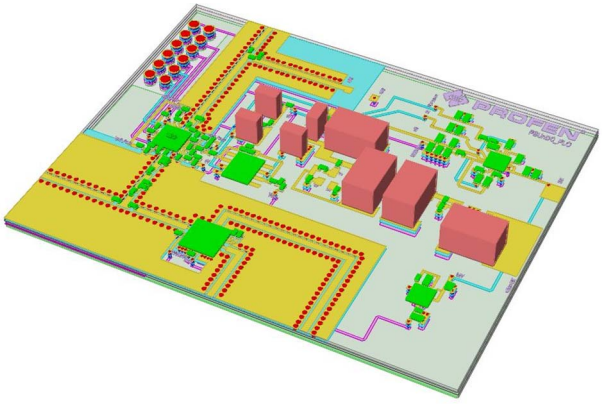

Figure 6. 3D design of the proposed phase-locked loop circuit and reference oscillator card.

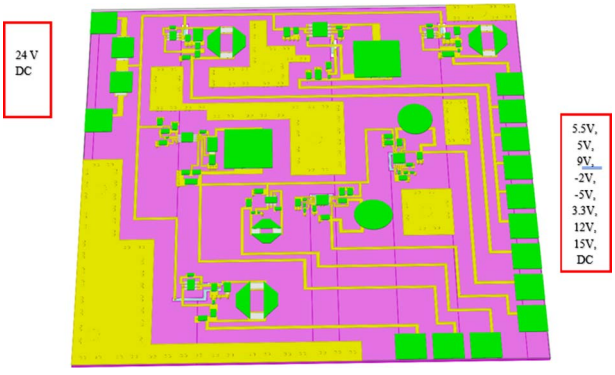

Figure 7. Layout of bias network of the RF block.

detector, (iii) making serial peripheral interface (SPI) communication with a PLL synthesizer, (iv) setting the operating sequence of switching power supplies, (v) to control RF mute mode, (vi) sending power and attenuation information on the circuit to different circuit boards via serial communication.

Mechanical design

According to the results of thermal and electromagnetic simulations of the designed RF circuits, the mechanical design of the RF circuit boxes has been made to minimize the negative effects that may arise from thermal and electromagnetic interaction due to system integration. The product will be outdoor equipment. Figures 8(a) and 8(b) show the images of the front and rear panels of the designed mechanical box designed on Solidworks. The frequency down-converter will be mechanically enclosed in a Rack type 2U box.

Simulation and measurement results

In Figure 9(a), the Nucleo card is the control card that will control the attenuator, SPI communication with the PLL card, control of the power detector output, and mute mode operation. This control card has been managed with an ethernet connection interface by performing the necessary software studies.

The regulator card in the frequency down-converter is fed with different DC voltage values: 18–32 V DC input regulator card. It meets the DC supply requirement of the frequency down-converter (5 V, 9 V, −5 V, −2 V, 15 V, 12 V, 5.5 V, 9 V, 3.3 V). The input of the frequency down inverter will be 220 V AC. 220 V AC voltage is reduced to AC 220 V, DC 24 V with LRS-100-24 of Mean Well.

The PLL board is the circuit in which we perform the locking process in the frequency range of 7280 MHz and 7780 MHz for the LO input of the RF board. This circuit uses a 10 MHz VCTCXO crystal oscillator, and frequency stability and depreciation year are ± 1 ppm.

RF card is a circuit consisting of RF input, IF output, input test port, output test port, and power detector output, as shown in Figure 9(b). At the IF output, two low-pass filters suitable for the output frequency are used. A four-way splitter is used in the output test port. The purpose here is to give the test port output and power detector output. The measurement setup is shown in Figure 9(b).

The Nucleo card is the control card that will control the attenuator, SPI communication with the PLL card, control of the power detector output, and mute mode operation.

This control card has been managed with an ethernet connection interface by performing the necessary software studies. The

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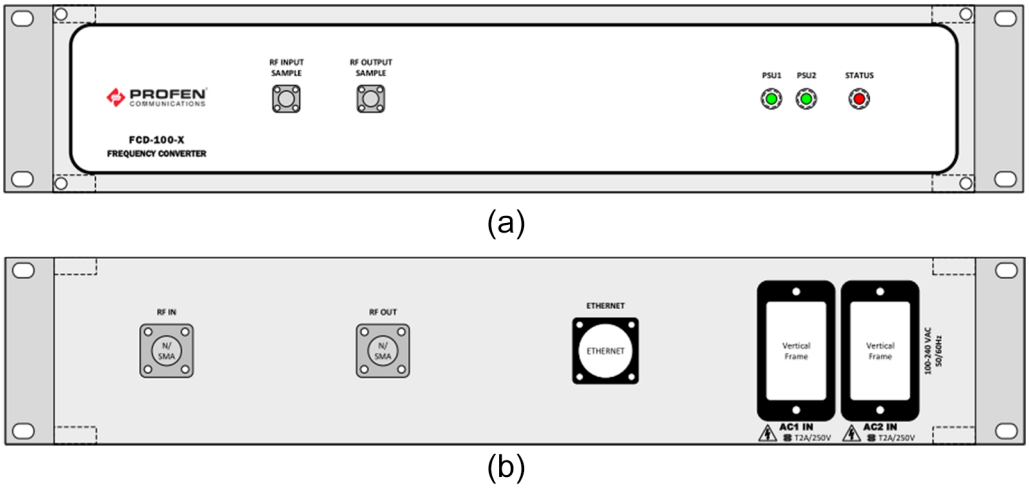

Figure 8. (a) The front panel view of the proposed X-band frequency down-converter box design and (b) the back panel view of the proposed X-band frequency down-converter box design.

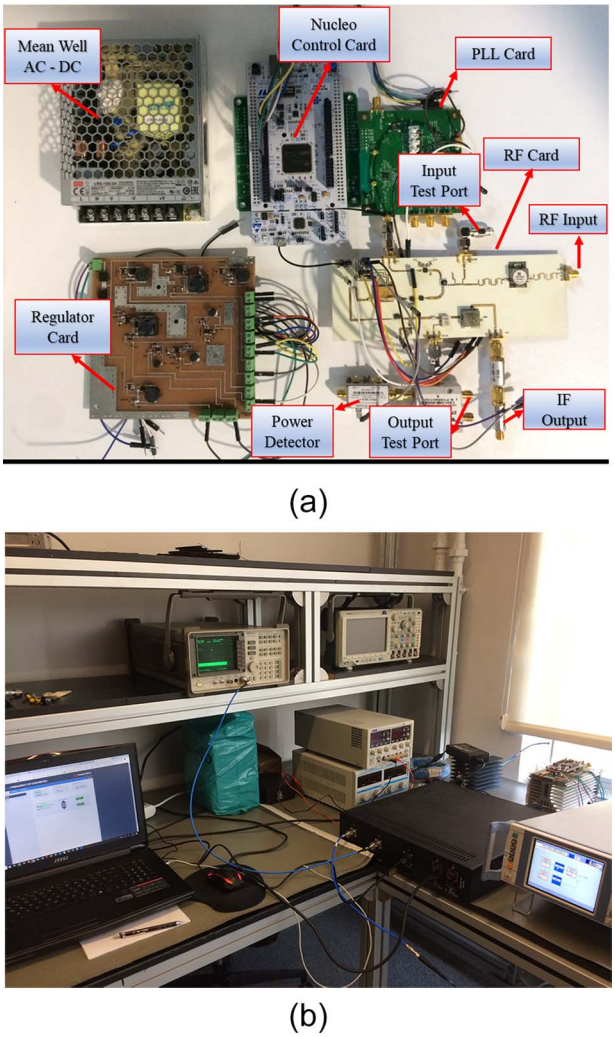

Figure 9. (a) The circuit design of the proposed frequency down-converter and (b) the measurement setup of proposed X-band frequency down-converter.

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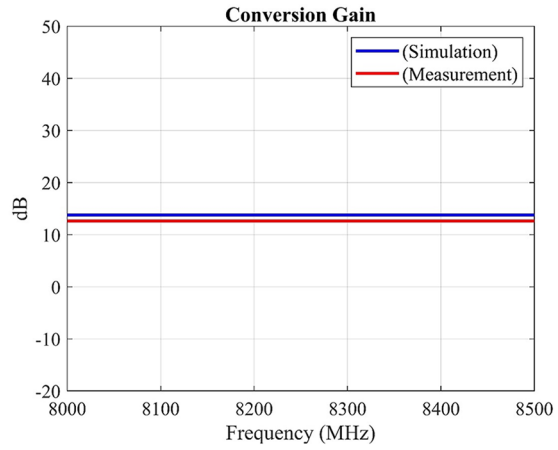
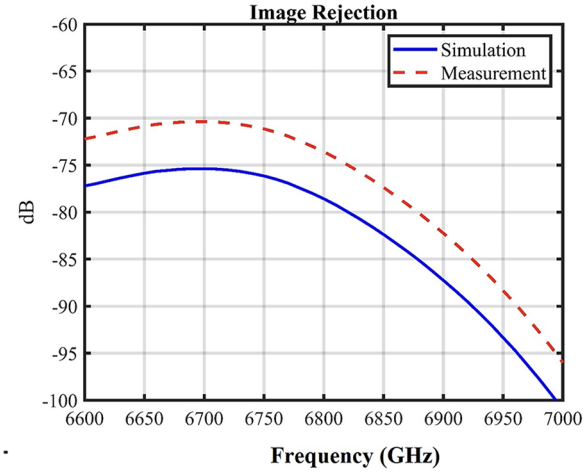
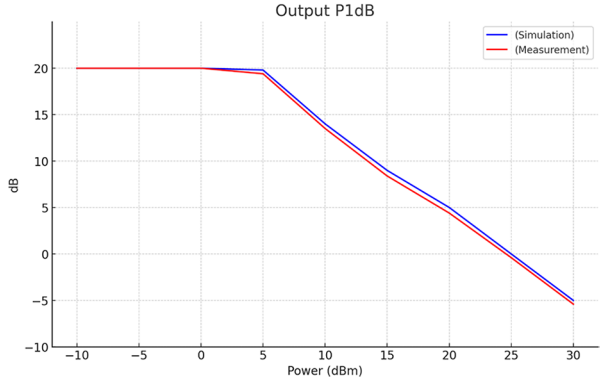


(a)



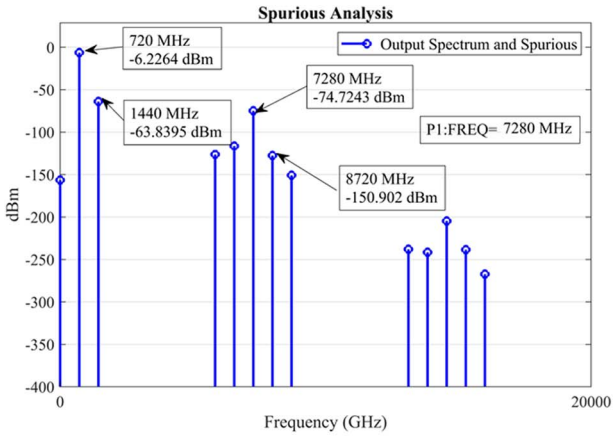
(b)



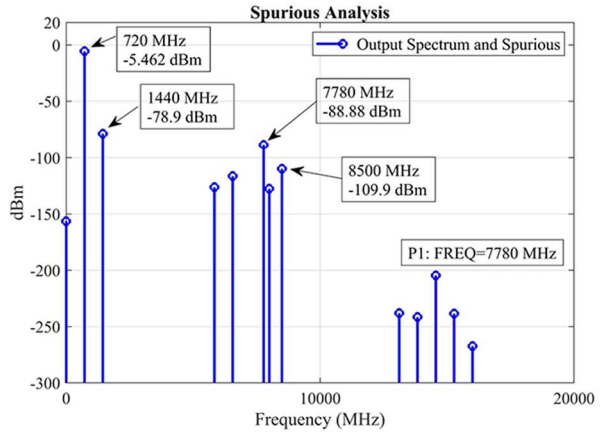
(c)

Figure 10. (a) Measurement and simulation results of in-band gain of the down-converter for LO: 7780 MHz, (b) measurement and simulation results of the image rejection of the down-converter, and (c) measurement and simulation of the P1dB point of the down-converter.

input frequency range of the designed X-band frequency down-converter system is between 8 and 8.5 GHz. The output frequency band is at 720 MHz center frequency with ±200 MHz bandwidth.



(a)



(b)

Figure 11. (a) Measurement result of the single harmonics at the input and spurious signals LO: 7280 and (b) measurement result of the single harmonics at the input and spurious signals LO: 7780.

According to the X-band frequency down-converter design simulation and measurement results, the in-band gain value for LO power 7 dBm is shown in Figure 10(a) for LO frequency 7280 MHz. According to the simulation results, the loop gain in the operating band is 14 dB close to the measurement results which is equal to 13.7 dB.

Figure 10(b) shows the image rejection graph of the frequency down-converter. When the image rejection frequencies of the mixer are calculated, the frequency band 6560–7060 MHz is where the image frequencies are located. The 70 dB value given in the target specification is met according to the simulation result. A cascade band-pass filter of our design was used where the RF input is located to obtain this result. Thus, a value even lower than the desired value was obtained.

The P1dB point of the system, shown in Figure 10(c), simulation result is 13.9 dBm, and it meets the measurement result which is equal to 13.86 dBm.

The phase noise measurement of the frequency down-converter. In the measurement, the M1 and M2 are −3 dBm and −49.79 dBm, respectively. The difference between these points is −46.79 dBc. In the spectrum analyzer, Resolution Bandwidth (RBW) is 300 Hz, and Video Bandwidth (VBW) is 300 Hz.

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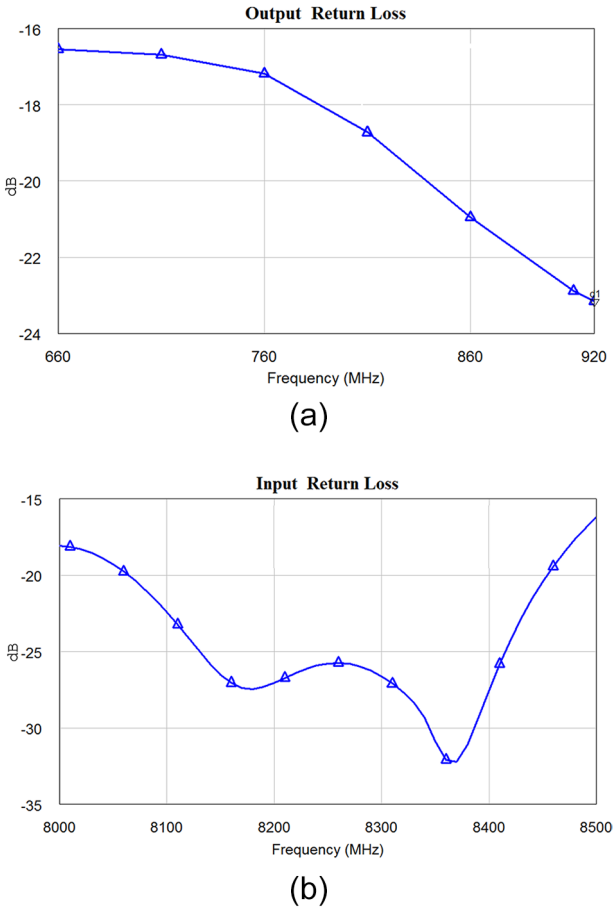

Figure 12. (a) Measurement result of the input return loss of proposed X-band down-converter and (b) measurement result of the output return loss proposed X-band down-converter.

The phase noise value is −46.79 dBc + (−27.4 dBc): −74.2 dBc/Hz at 100 Hz.

Figure 11(a) shows the in-band and out-of-band spurious signals when the input power is given at −20 dBm. In the given graph, the spurious level is below −74.7 dBm when LO is at 7280 MHz frequency. Since the X-band frequency down-converter will be directly on the communication line, the spurious level becomes more critical. The simulation result suits in-band, out-of-band, and LO leakage levels. In the same case, in the graph in Figure 11(b), when LO is at 7780 MHz frequency, the spurious level is below −88.8 dBm, both in-band and out-of-band.

In the graphs given in Figures 12(a) and 12(b), the input and output return loss is below −15 dB. It meets the minimum value given in the target specification. S-parameter measurements were taken using vector network analysis at a LO frequency of 7280 MHz. Input return loss was considered for RF input, and measurements were taken assuming IF output for output return loss. The X-band frequency down-converter system uses couplers at the input and output. Thanks to these couplers, the input and output frequency will be monitored and adjusted. The microcontroller circuit will manage the RF log detector at the coupling end of the coupler. The gain will be monitored and adjusted by using a 6-bit digital attenuator. The digital attenuator can also be adjusted in 1 dB steps between the desired ±20 dB by using the microcontroller circuit. The RF output cancellation feature is a process that can be done by cutting the regulator used. This process can be intervened through the microcontroller using the digital attenuator.

Conclusion

Ground stations are part of any satellite network, providing communication with satellites. The communication quality depends on the performance of the satellite ground station and the satellite. LEO satellites are also used for public communication and scientific purposes. LEO satellites generally communicate with ground stations at S-band and X-band. The front-end circuit after the LNA in the downlink section is the frequency down-converter. The frequency down-converter is used in the ground station and terminals of satellite communication systems since communication at high frequencies in free space needs to be down-converted before receiver input. The output return loss is between −16 dB and −24 dB, and the input return loss is between −15 dB and −35 dB in the operation frequency range.

Finally, target specifications which are seen in Table 1 such as conversion gain, PdB1, image rejection, phase noise, LO leakage meet the simulation results with minor changes.

Direct conversion has given the frequency down-converter optimum performance. According to the literature, it is difficult to provide such high performance at near LO and RF frequencies in terms of frequency, but we have succeeded in doing so with our design.

In the sparse number of experiments that are currently accessible in the literature [20]–[26], double conversion are employed to reduce the broadband frequency. The effect of this wide range on the performance of the solution with direct conversion is not much mentioned in the literature. But in the contribution of our study, we do this in a creative and effective manner across a very broad spectrum using a direct conversion.

In this study, a single LO mixer stage is used to get the optimum performance in the frequency down-converter. According to the literature, it is difficult to provide such high performance at near LO and RF frequencies in terms of frequency, but we have succeeded in doing so with our design.

Data availability statement. The data used to support the findings of this study are available from the corresponding author upon reasonable request.

Competing interests. The authors declare that there are no conflicts of interest regarding the publication of this paper.

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