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Application of Electron Tomography for Semiconductor Device Analysis

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The continual shrinking of semiconductor devices has resulted in commercial products with complex non-planar features and dimensions comparable to or smaller than the thickness of a typical TEM specimen. As a result, device features and defects are becoming increasingly difficult to image and accurately identify by conventional cross-section (S)TEM imaging due to geometric blurring in a single 2D projection. With the development of even smaller devices, this limitation will become even more pronounced in the next years. TEM and STEM tomography are proving to be a promising solution to this problem by offering a high-resolution 3-dimensional image of the volume of interest. We will demonstrate some of the possibilities and also limitations of TEM and HAADF-STEM tomography to accurately image the 3D structure of semiconductor devices. Application examples will include high-aspect ratio VIAs [1], DRAM [1] and flash memory devices [2].

In high-aspect ration VIAs, local variations of the barrier layer and copper seed layer thickness can be imaged easily by HAADF-STEM tomography (Fig. 1). The resulting data can be used to identify defects and voids in the VIA and measurements can be performed in 3D. Significantly more challenging is the analysis of DRAM or flash memory devices by electron tomography as materials with extreme density differences (e.g. tungsten vs. silicon and silicon oxynitride) need to be imaged simultaneously. Therefore, special attention has to be paid to the quality of the reconstruction and how reconstruction artifacts, e.g. due to the 'missing wedge', affect the validity and interpretation of the data. Nevertheless, using appropriate imaging and reconstruction conditions, it is possible to e.g. image 1.5 nm silicon oxynitride layers in the gate of a DRAM in close proximity to tungsten contacts (Fig. 2). Together these application examples highlight the usefulness of this technique, but also show the importance of correct interpretation to avoid errors due to reconstruction artifacts.

References:

[1] C. Kübel, S. Kujawa, J.-S. Luo, H.-M. Lo, J. D. Russell '*Application of Electron Tomography for Semiconductor Device Analysis*' in '*8th International Workshop of Stress-Induced Phenomena in Metallization'*, edited by E. Zschech, AIP Conference Proceedings 817 (2006). American Institute of Physics, Melville, New York, in print.
[2] C. Kübel, et al. '*Recent Advances in Electron Tomography: TEM and HAADF-STEM Tomography for Materials Science and Semiconductor Applications',* Microscopy and Microanalysis (2005) **11**(5), p. 378-400.

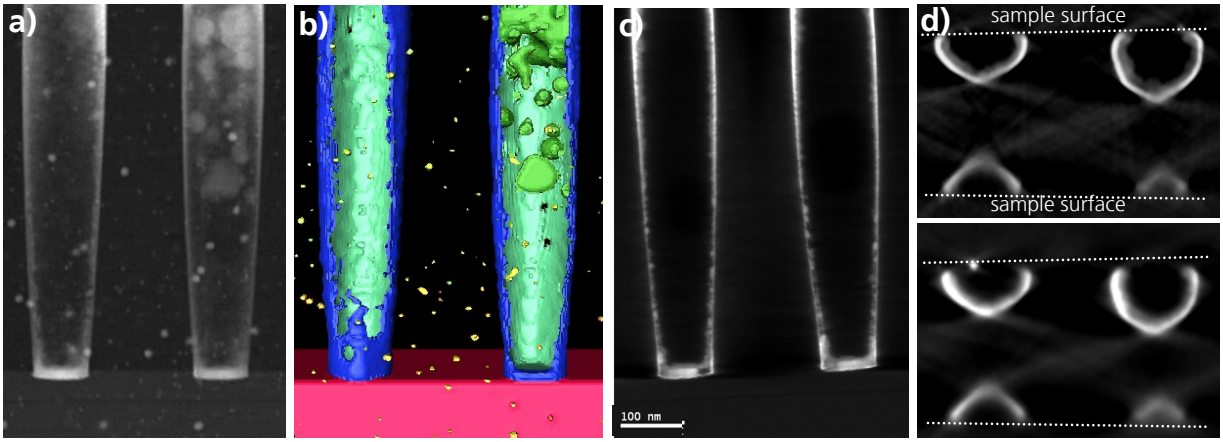

Figure 1: a) HAADF-STEM image and b) surface rendering of an unfilled VIA.
c) Slice through the reconstructed volume parallel and d) perpendicular to the TEM sample surface revealing the barrier layer thickness and variations in the copper seed coverage.

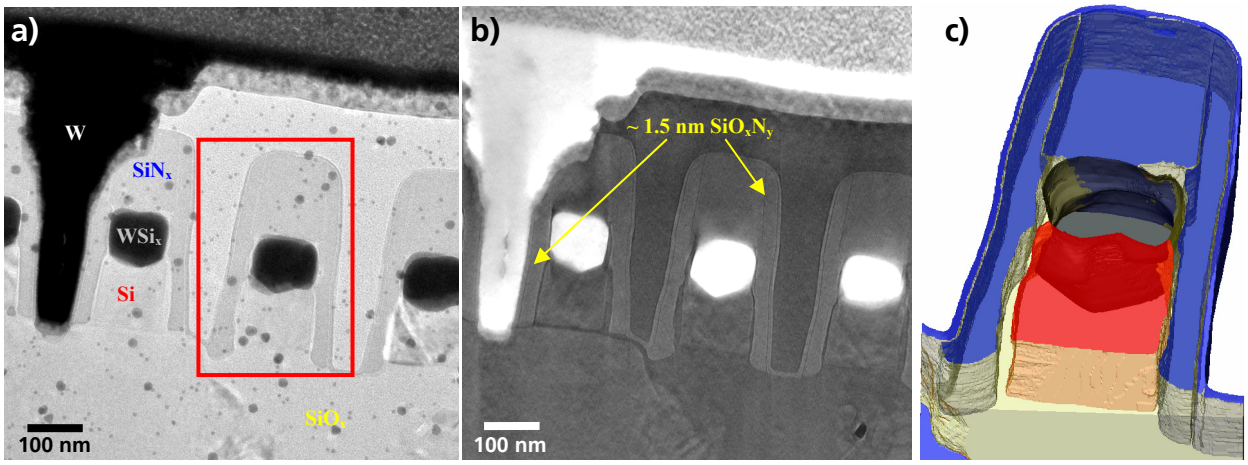

Figure 2: a) TEM image of a DRAM with contact and gates;
b) Slice through the reconstructed volume show e.g. 1.5 nm silicon oxynitride layers in the gate;
c) Surface rendering of the central gate based on the 3D reconstruction.

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