






Four-element LC-baluns for power matching arbitrary impedances

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Research Paper

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Abstract

Six four-element balun topologies are introduced that enable complex impedance matching in addition to common-mode rejection. Design equations for these topologies are presented. Three of these networks are universal, while the other three are capable of performing only specific impedance transformations. Examples of these networks were designed and fabricated along with a traditional lattice balun network for an operating frequency of 300 MHz. These networks were verified through extensive electromagnetic simulations and by measuring the fabricated networks. The fabricated novel network examples were able to achieve common-mode rejection ratios above 20 dB, power wave reflection coefficients below -20 dB, and insertion losses of approximately 0.1 dB; these results were similar to or better than the performance of the fabricated traditional lattice balun. The design example networks also provided power matching and low insertion loss over a greater bandwidth compared to the fabricated traditional network. These networks will allow for the footprints of lumped-element balun circuitry to be reduced, which is particularly useful in integrated circuit design. These topologies are also expected to further increase radio-frequency (RF) circuit design flexibility by offering more alternative realizations.

Introduction

Baluns are needed to properly interface balanced devices such as balanced antennas and MRI detectors to unbalanced devices and components such as single-ended amplifiers and coaxial cables. Lumped-element baluns are used in situations where baluns based on transmission lines would be infeasible, due to their large size. A commonly used four-element balun topology is the LC lattice balun, which uses two inductors and two capacitors in a lattice configuration [1]. Other lumped-element balun topologies have been introduced, such as LCCC baluns [2], second-order lattice baluns [3], and compensated high/low-pass baluns [4]. These baluns are generally only able to match real impedances, and thus they require extra elements to cancel the imaginary parts of the impedances that they are matching. There exist lumped-element topologies for matching complex impedances, though these generally either use transformations from coupled-line designs [5] or modifications of existing lumped-element balun topologies [6]. As a result, these baluns consist of a greater number of components compared to the traditional lattice balun.

This paper describes six passive balun topologies containing four reactive lumped elements and are capable of power matching arbitrary complex impedances on the balanced and unbalanced ports simultaneously. Fritz et al. [7] have previously described a four-element balun that resembles the extended T topology in this paper and derived design equations for complex impedance matching. Bradley and Frank [8] have also considered a special case of the extended Pi network, which this paper investigates further by generalizing it for complex impedance matching. One of these topologies uses a lattice shape that is not required to be symmetrical. Apel and Page [9] have presented a balun that uses an asymmetric lattice topology, which this paper generalizes for complex impedance matching by considering other component combinations that can be used for the lumped elements. A traditional lattice balun and an example novel four-element balun for complex impedance matching are shown in Figure 1 for illustration. In theory, the novel networks are able to provide the same common-mode rejection and power matching as traditional networks.

Reducing the number of elements required for a lumped-element power matching network may lessen the effects of lossy and noisy elements. This also enables these new balun topologies to be directly integrated with matching networks to reduce their overall footprints, which can be particularly useful in integrated circuit design. In addition, the RF circuit designer has

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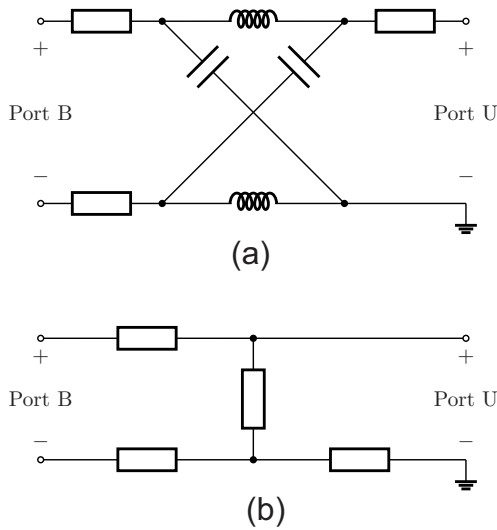


Figure 1. (a) LC lattice balun extended to match complex impedances and (b) novel Yu network balun.

the possibility of choosing among several balun topologies, which can be an advantage if the availability of some LC component values is limited, further increasing design flexibility.

Derivation process

Summary

Common-mode rejection and two-port power matching were the two criteria used to evaluate potential power-matching balun topologies. Three- and four-element network topologies were exhaustively investigated to determine if their reactances could be chosen such that these criteria could be simultaneously satisfied. The topologies were also constrained to be lossless and reciprocal, thus the impedances of the elements were modeled as purely imaginary. Lcapy [10] was utilized to symbolically analyze networks and to determine design equations for the constituent components. Jupyter notebooks detailing the derivation of these design equations are available in the supplementary material at [11]. The derivation process involved the following steps:

- (i) Model the network topology as a SPICE netlist and create two- and three-port models using the netlist.
- (ii) Using the impedance matrix of the three-port model, obtain the three-port scattering parameters for the network.
- (iii) Obtain symbolic expressions for the common- and differential-mode response of the network, and thus an expression for the inverse of the common-mode rejection ratio (CMRR) in terms of the element reactances.
- (iv) Solve for the element reactances such that the inverse of the CMRR is zero.
- (v) Ensure power matching by solving for the remaining element reactances such that one port is conjugate matched or such that the two-port impedance parameters provide power matching.
- (vi) Substitute reactances solved from step (v) into the expressions solved from step (iv).
- (vii) Manually simplify the expressions to yield useful design equations.

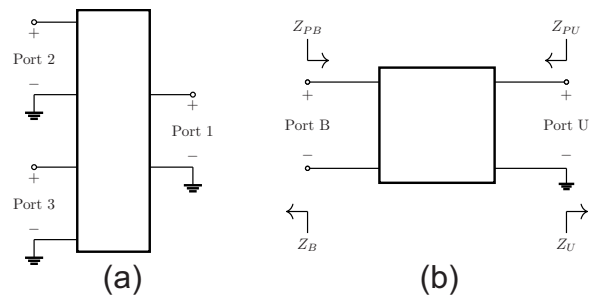


Figure 2. (a) Three-port and (b) two-port models of balun topologies.

The derivation process involved two steps that use a symbolic solver, these steps were separated due to limitations of the symbolic solver used. The process of converting the symbolic representation of the three-port impedance matrix to three-port scattering parameters was manually implemented, and this implementation used the process described by Kurokawa [12]. The last step of manually simplifying the expressions returned by the symbolic package was required to express the design equations in a useful form that used \pm operators.

Common-mode rejection

Common-mode rejection refers to the extent to which a differential device attenuates common-mode signals between its ports. For a balun, common-mode rejection is used to ensure that common-mode signals on the balanced port do not propagate to the unbalanced port.

To model common-mode rejection, potential balun topologies were modeled as three-port networks, with the balanced port being split into two single ended ports referenced to the ground on the unbalanced port as depicted in Figure 2(a). For this model, the reference port impedance of port 1 is the unbalanced port impedance, and the reference port impedances of ports 2 and 3 are half of the balanced port impedance.

The three-port scattering parameters can thus be used to compute the differential and common-mode responses using (1) and (2), respectively. Using these values, the CMRR can be determined from (3) [13]

$$S_{21ds} = \frac{S_{21} - S_{31}}{\sqrt{2}} \tag{1}$$

$$S_{21cs} = \frac{S_{21} + S_{31}}{\sqrt{2}} \tag{2}$$

$$CMRR = \left| \frac{S_{21ds}}{S_{21cs}} \right| \tag{3}$$

An ideal balun would have an infinite CMRR; hence, one of the criteria used to evaluate potential balun topologies was that the reciprocal of the CMRR is 0.

Power matching

Power matching or conjugate matching involves configuring the source and load impedances in a network to ensure that the maximum power is transferred from the source to the load. For a network to be power matched, the load impedance must be the complex conjugate of the source impedance. Figure 2(b) presents how balun topologies were modeled as two-port networks for their

differential-mode operation. Z_{PB} and Z_{PU} refer to the impedances looking into the balanced and unbalanced ports of the balun, respectively. Likewise, $Z_B = R_B + jX_B$ and $Z_U = R_U + jX_U$ are the impedances that the balun is designed to match on the balanced and unbalanced ports, respectively. For power matching, $Z_{PB} = Z_B^*$ and $Z_{PU} = Z_U^*$, where a superscript asterisk refers to the complex conjugate of a quantity.

The power wave reflection coefficients at the balanced and unbalanced ports of the two-port network model of a balun are shown in (4a) and (4b), respectively [12]

$$\rho_B = \frac{Z_{PB} - Z_B^*}{Z_{PB} + Z_B} \tag{4a}$$

$$\rho_U = \frac{Z_U - Z_{PU}^*}{Z_U + Z_{PU}} \tag{4b}$$

A port being conjugate matched implies that its corresponding power wave reflection coefficient is 0. For lossless and reciprocal networks, $|\rho_B|^2 = |\rho_U|^2$. Therefore, if one port is conjugate matched, the other will also be conjugate matched. For evaluating potential balun topologies, it is thus sufficient to only constrain the network such that one port is conjugate matched.

Balun topologies and design equations

Six four-element lossless reciprocal network topologies were found that are capable of common-mode rejection and power matching arbitrary complex impedances. One of these topologies has the same shape as a traditional lattice balun, though it is not symmetrical in general. These topologies are displayed in Figure 3.¹

The corresponding design equations are shown in Table 1. X_i refers to the reactance of the lossless lumped element Z_i . In general, each topology has two solutions for any given inputs. The two solutions for the lattice topology correspond to the terminals of the balanced port being reversed, and thus only one solution is presented. In this paper, the solution for a topology where \pm is replaced by a + is referred to as the first solution, and the other solution is referred to as the second solution. Lumped elements can be implemented with capacitors and inductors by using the reactances and operating frequency to calculate their capacitances and inductances. A Jupyter notebook and associated Python package were developed to compute the component values for matching networks given values for Z_B, Z_U , and the operating frequency [11].

The general design equations for the Dipper, Yu, and Reverse Yu topologies are only valid for certain impedance transformations. An extra parameter, Δ , has been introduced for these topologies to simplify the design equations. These topologies can also only be constructed for impedance transformations that correspond to $\Delta \geq 0$, for their Δ parameter. If these constraints are not satisfied, the design equations will yield values for the component reactances that are not real, which violates the assumption that the networks are lossless.

There exist three-element power matching baluns for some specific impedance transformations. If X_3 for the Extended T topology is close to 0, then X_1 for the Extended Pi topology, and X_1 or X_3 for the lattice topology approach infinity. X_4 for the Dipper topology

¹The Extended T and Extended Pi networks resemble T and Pi networks with one added element. The Yu and Reverse Yu networks resemble the katakana character “yu” (ユ). The Dipper network resembles the “Big Dipper” asterism.

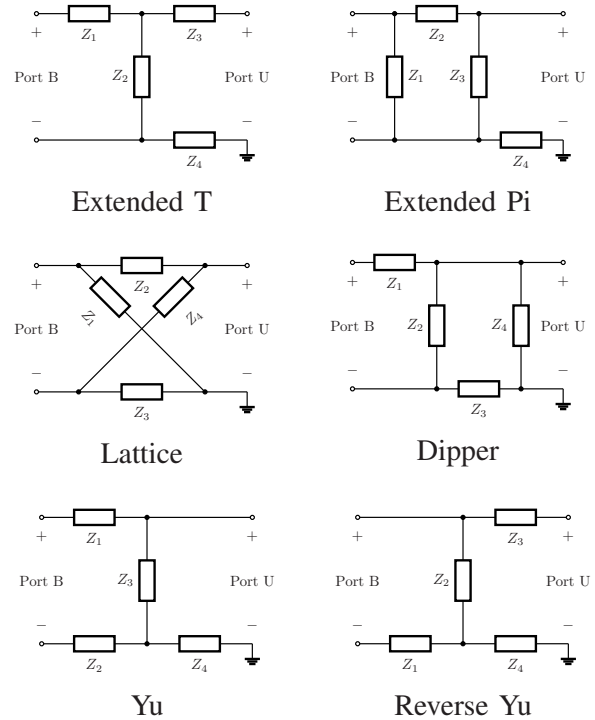


Figure 3. Four-element balun topologies.

and X_2 for the Yu topology also approach infinity and 0, respectively. If sufficiently small and large reactances are replaced with short- and open-circuits, respectively, the remaining elements in these topologies converge to the same solution. Another three-element special case exists where X_1 for the Yu topology and X_3 for the Reverse Yu topology approach 0. In this case, these two topologies converge to a network resembling an upside-down T network.

The design equations for the Dipper, Yu, and Reverse Yu topologies also cannot be directly applied in the case where $R_B = 4R_U$. In this case, there is only one solution for these topologies and the limit of the design equations must be used instead. Table 2 displays the design equations for the Dipper, Yu, and Reverse Yu topologies for this special case. The design equations also imply that some of the topologies have DC characteristics that may be desirable for some applications, for example, DC blocking and DC feeding. These DC characteristics only manifest for certain impedance transformations.

Experimental comparison to traditional circuits

Design procedure

The design process for the balun networks entails the following steps:

- (i) Identify balanced and unbalanced port impedances, Z_B and Z_U , and calculate the ideal reactances for the elements using the design equations in Table 1 or Table 2.
- (ii) Calculate capacitances and inductances that match the ideal reactances at the chosen frequency.
- (iii) Choose the desirable technology for practical implementation and realize the design.

Table 1. Design equations for balun topologies

Topology	Design equations
Extended T	$X_1 = \mp Z_B \sqrt{\frac{R_U}{R_B}}$
	$X_2 = \pm Z_B \sqrt{\frac{R_U}{R_B}}$
	$X_3 = \frac{R_U X_B}{R_B} - X_U \mp \frac{ Z_B }{2} \sqrt{\frac{R_U}{R_B}}$
	$X_4 = \mp \frac{ Z_B }{2} \sqrt{\frac{R_U}{R_B}}$
Extended Pi	$X_1 = \frac{2 Z_B ^2 R_U}{2X_U R_B - 2R_U X_B \mp Z_B \sqrt{R_U R_B}}$
	$X_2 = \pm Z_B \sqrt{\frac{R_U}{R_B}}$
	$X_3 = \mp Z_B \sqrt{\frac{R_U}{R_B}}$
	$X_4 = \pm \frac{ Z_B }{2} \sqrt{\frac{R_U}{R_B}}$
Lattice	$X_1 = \frac{R_U Z_B ^2}{2R_B X_U - 2R_U X_B - Z_B \sqrt{R_U R_B}}$
	$X_2 = Z_B \sqrt{\frac{R_U}{R_B}}$
	$X_3 = \frac{R_U Z_B ^2}{2R_B X_U - 2R_U X_B + Z_B \sqrt{R_U R_B}}$
	$X_4 = - Z_B \sqrt{\frac{R_U}{R_B}}$
Dipper	$\Delta = 4 Z_U ^2 - R_U R_B$
	$X_1 = -\frac{X_B}{2} \mp \frac{\sqrt{R_B \Delta}}{2\sqrt{R_U}}$
	$X_2 = \frac{X_B}{2} \pm \frac{\sqrt{R_B \Delta}}{2\sqrt{R_U}}$
	$X_3 = -\frac{X_B}{4} \mp \frac{\sqrt{R_B \Delta}}{4\sqrt{R_U}}$
	$X_4 = \frac{R_U Z_B ^2 (R_B - 4R_U)}{X_B + 4X_U - \frac{4R_U X_B}{R_B} \pm \sqrt{\frac{R_B \Delta}{R_U}}} - X_U - \frac{R_U X_B}{R_B}$
Yu	$\Delta = 4 Z_U ^2 - R_U R_B$
	$X_1 = -\frac{X_B}{2} \pm \frac{\sqrt{R_B \Delta}}{2\sqrt{R_U}}$
	$X_2 = \frac{2R_B X_U}{4R_U - R_B} - \frac{X_B}{2} \mp \frac{\sqrt{R_B^3 \Delta}}{(8R_U - 2R_B)\sqrt{R_U}}$
	$X_3 = \frac{2R_B X_U \mp 2\sqrt{R_U R_B \Delta}}{4R_U - R_B}$
	$X_4 = \frac{-R_B X_U \pm \sqrt{R_U R_B \Delta}}{4R_U - R_B}$
Reverse Yu	$\Delta = Z_B ^2 - 4R_U R_B$
	$X_1 = \frac{-2R_U X_B \mp \sqrt{R_U R_B \Delta}}{4R_U - R_B}$
	$X_2 = \frac{-2R_U X_B \mp \sqrt{R_U R_B \Delta}}{4R_U - R_B}$
	$X_3 = -X_U \mp \frac{\sqrt{R_U \Delta}}{2\sqrt{R_B}}$
	$X_4 = \frac{2R_U X_B \pm \sqrt{R_U R_B \Delta}}{8R_U - 2R_B}$

Design examples

The design process of the novel balun topologies is illustrated by fabricating chosen example solutions. The anticipated scenario for this demonstration is a dipole antenna, with $Z_B = 73 + 43j\Omega$,

Table 2. Design equations for the Dipper, Yu, and Reverse Yu networks for $R_B = 4R_U$

Topology	Design equations
Dipper	$X_1 = 2X_U - \frac{X_B}{2}$
	$X_2 = \frac{X_B}{2} - 2X_U$
	$X_3 = X_U - \frac{X_B}{4}$
	$X_4 = \frac{ Z_U ^2 (4X_U - X_B)}{4R_U^2 - 4X_U^2 + 2X_B X_U}$
Yu	$X_1 = 2X_U - \frac{X_B}{2}$
	$X_2 = X_U - \frac{R_U^2}{X_U} - \frac{X_B}{2}$
	$X_3 = -X_U - \frac{R_U^2}{X_U}$
	$X_4 = \frac{ Z_U ^2}{2X_U}$
Reverse Yu	$X_1 = \frac{-4R_U^2}{X_B} - \frac{X_B}{4}$
	$X_2 = \frac{-4R_U^2}{X_B} - \frac{X_B}{4}$
	$X_3 = \frac{X_B}{4} - X_U$
	$X_4 = \frac{2R_U^2}{X_B} + \frac{X_B}{8}$

being matched to a coaxial cable, with $Z_U = 75\Omega$, in a radio-frequency system. In addition, numerical verification for full complex impedance cases ($Z_B = 50 + 100j\Omega$, $Z_U = 30 + 80j\Omega$, and several others, as listed in Table A1) was also performed as described in Appendix A. The design frequency in this example is 300 MHz.

The second solution of the Extended Pi topology and the second solution of the Yu topology were chosen for demonstration as they required fewer inductors compared to the other solutions, which could result in lower losses. A traditional lattice network was also designed for comparison. The capacitance of $C_1 \approx 89.22$ fF in the Extended Pi network was sufficiently small that it was implemented as an open-circuit, resulting in the network being effectively implemented as a three-element network. This three-element network approximately converges with the first solutions of the Extended T and Dipper networks, and the lattice network. Passive Plus 1111 capacitors and Coilcraft 1206 inductors were used to construct the networks. Non-ideal effects were accounted for by ensuring the selected components resulted in each element having approximately the same reactance as its ideal form. Figures 4, 5, and 6 present the ideal and realized forms of these networks.

Methods

The design examples were constructed on printed circuit boards (PCBs) using a lumped-element realization at low frequencies, though the topologies described can be used with an integrated realization that can function for frequencies in the gigahertz range. PCBs were designed for each example network, such that their three-port parameters could be verified. The PCBs were designed for 1.6 mm FR4 substrate with copper traces.

Initial verification was performed using electromagnetic co-simulations in Keysight Advanced Design System (ADS) Momentum. These simulations are detailed in Appendix B. The

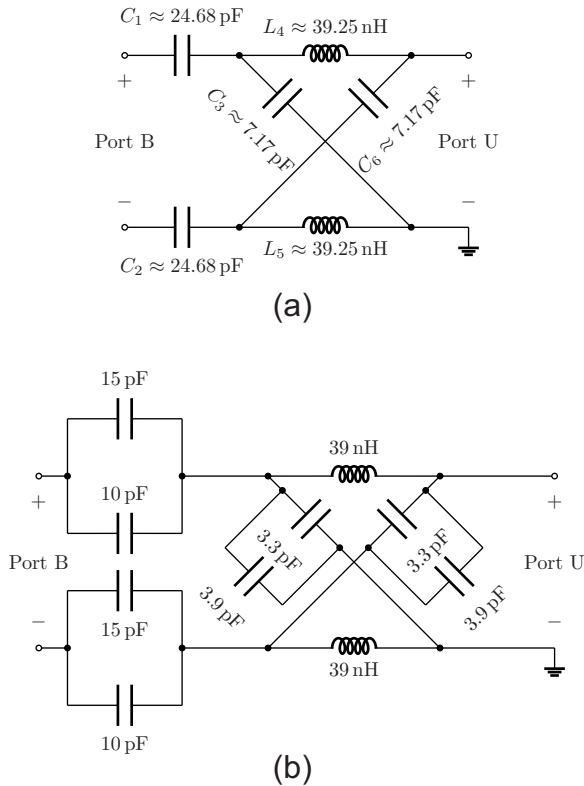


Figure 4. (a) Ideal traditional lattice balun and (b) implemented traditional lattice balun.

networks were then fabricated such that their three-port parameters could be measured. Figure 7 shows the fabricated forms of the networks.

The three-port parameters of the fabricated networks were determined by measuring the two-port parameters for each pair of ports with the remaining port terminated with a $50\ \Omega$ load. The measurements were performed with a Rohde & Schwarz ZNL3 Vector Network Analyzer. The two-port measurements were then combined to yield the three-port scattering parameters by employing the technique described by [14]. A Jupyter notebook was created to assist with this procedure [11]. ADS simulations were then performed on the resulting three-port parameters to calculate the differential two-port parameters and CMRRs. Appendix B describes this process in detail.

Results

The CMRRs of each network were determined to confirm that they are able to effectively reject common-mode currents. Figure 8 shows the CMRR for the Momentum co-simulation and experimental measurements of each network.

The power wave reflection coefficient at the balanced port and the insertion loss for each circuit were also determined. Figure 9 presents these quantities for each network.

Discussion

The results in Figure 8 demonstrate that the fabricated novel balun network prototypes are able to achieve a similar or greater level of common-mode rejection compared to a traditional lattice

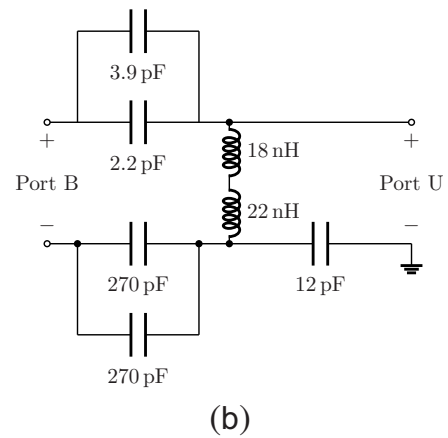
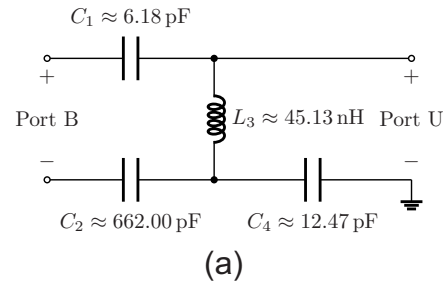


Figure 5. (a) Ideal Yu solution 2 balun and (b) implemented Yu solution 2 balun.

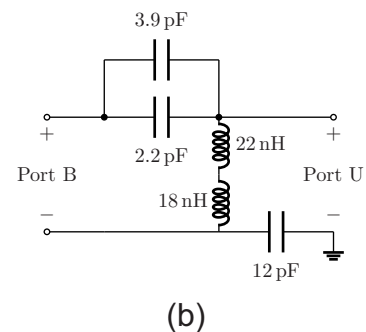
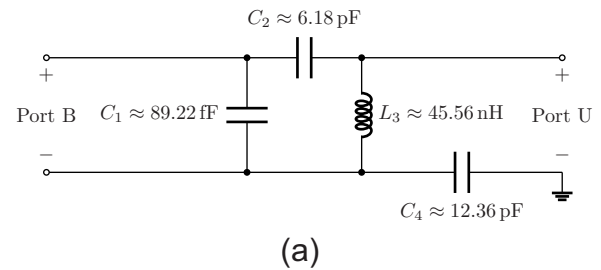


Figure 6. (a) Ideal extended Pi solution 2 balun and (b) implemented three-element balun.

balun, with the novel three-element network having the greatest measured CMRR at the design frequency. A greater level of common-mode rejection may be achievable if parasitic effects are reduced or compensated for. If ideal components are used with a sufficient number of significant figures for component values,

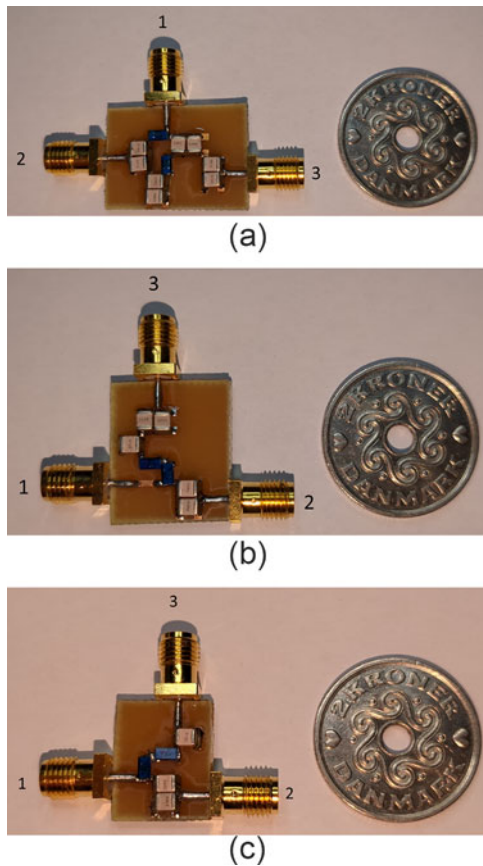


Figure 7. Fabricated PCBs for the example (a) lattice, (b) Yu, and (c) three-element networks. Ports are annotated with their corresponding three-port port numbers. The dimensions of the lattice network PCB are 24.5 mm by 18.1 mm. The dimensions of the Yu network PCB are 20.9 mm by 17.9 mm. The dimensions of the three-element network PCB are 16.9 mm by 14.0 mm.

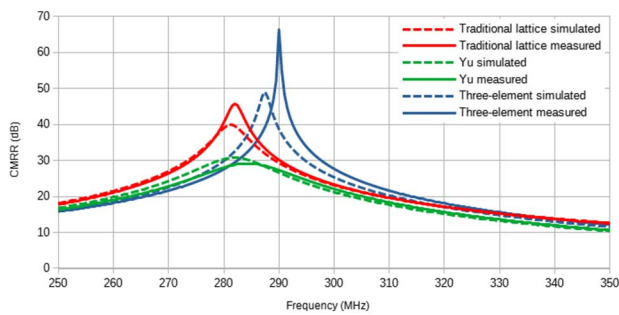
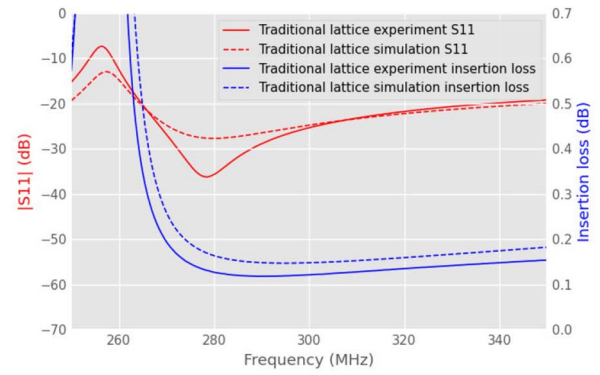


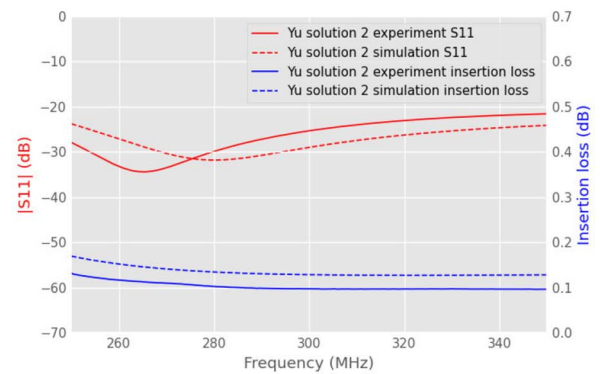
Figure 8. Measured and simulated common-mode rejection ratios of example balun networks.

traditional lattice and novel topologies yield infinite CMRR in simulations.

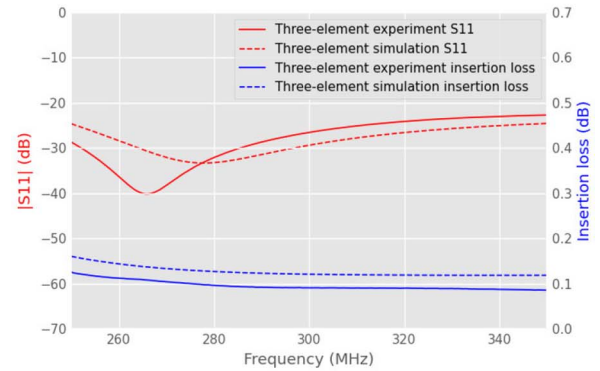
Figure 9 also indicates that the fabricated new network examples achieve improved power matching and insertion loss compared to a traditional lattice balun at the design frequency. The novel network examples also exhibit low insertion loss and power reflection over a greater bandwidth compared to the traditional lattice balun. The results in Figure 9 only provide an approximation of the broadband characteristics of the networks as it assumes that



(a)



(b)



(c)

Figure 9. Power wave reflection coefficient at the balanced port and insertion loss for the fabricated example (a) traditional lattice, (b) Yu, and (c) three-element networks.

the dipole impedance remains constant over the frequency range shown.

Conclusion

Six four-element balun topologies were presented that can provide power matching for complex impedances. The design equations for these networks have been derived, which imply that three of these networks are only valid for certain impedance transformations. These topologies have been evaluated through simulations

and experimental measurements, which have demonstrated that they are capable of providing common-mode rejection and power matching.

Two of the novel networks and a traditional lattice balun were fabricated for an example design scenario. Their scattering parameters were measured and used to confirm that the novel networks achieve similar or better power matching and common-mode rejection compared to a traditional balun topology. The novel networks also exhibit low insertion loss and power reflection over a greater bandwidth than a traditional lattice balun.

These networks provide a minimal method for using lumped-element networks for power matching balanced and unbalanced devices. Future research directions include investigating the DC characteristics and bandwidths of these balun topologies in more detail. It is also anticipated that this will facilitate further development for low noise balun circuitry in integrated microwave devices by means of reducing the footprint of circuitry for feeding radio-frequency circuitry.

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Competing interests. The author(s) declare none.

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Appendix A. Numerical verification

Keysight ADS was used to verify the topologies through circuit simulations of the networks for three test cases using models of realistic off-the-shelf components. A traditional lattice balun was also designed for each test case for comparison. The conditions for the test cases are shown in [Table A1](#).

The first test case was used to verify all of the solutions, and the values of Z_B and Z_U were chosen such that all of the topologies would be valid. The second test case was used to verify the Yu, Reverse Yu, and Dipper networks for the special case where they only have one solution. Only the Yu, Reverse Yu, Dipper, and traditional lattice networks were simulated for the second test case. The third test case was used to confirm that the other solutions were valid for the design example used for experimental verification. The Reverse Yu networks were not simulated for the third test case as they are not able to achieve the required impedance transformation. Akin to the experimental verification, the Extended T 1, Extended Pi 2, lattice, and Dipper 1 networks were implemented as the same three-element network for the third test case. The three-element, Yu 2, and traditional lattice networks were implemented as the same networks as for the experimental verification for the third test case.

Three-port and two-port simulations were performed for each network to determine their CMRRs, power matching, and insertion losses. Each network was designed using Coilcraft 1206 inductors and Passive Plus 1111 capacitors. The Coilcraft inductors were modeled using the Touchstone models from [15], and the Passive Plus capacitors were modeled as series RLC components using data from [16]. Components were selected to ensure that the reactance of the implementation of each element is approximately equal to that of its ideal counterpart.

The results from the circuit simulations were compiled as presented in [Figures A1, A2, and A3](#).

The results for the three-element, Yu 2, and traditional lattice networks for the third test case are different from the experimental verification as the circuit simulations do not account for parasitic effects when realizing the networks on a PCB. The circuit simulations generally yield improved CMRRs, power matching, and insertion losses compared to the experimental results. The traditional lattice network appears to perform significantly better compared to its experimental results, which is likely due to its PCB having more parasitic effects as it required more components to fabricate.

The results for each test case demonstrate that the novel balun networks are able to achieve similar common-mode rejection, insertion loss, and power matching to the traditional lattice balun. Overall, this verification indicates that all of the novel networks can function effectively as baluns for conjugate matching arbitrary complex impedances.

Table A1. Conditions for each simulated test case

Test case	Z_B (Ω)	Z_U (Ω)	Design frequency (MHz)
1	$50 + 100j$	$30 + 80j$	300
2	$40 + 100j$	$10 + 80j$	300
3	$73 + 43j$	75	300

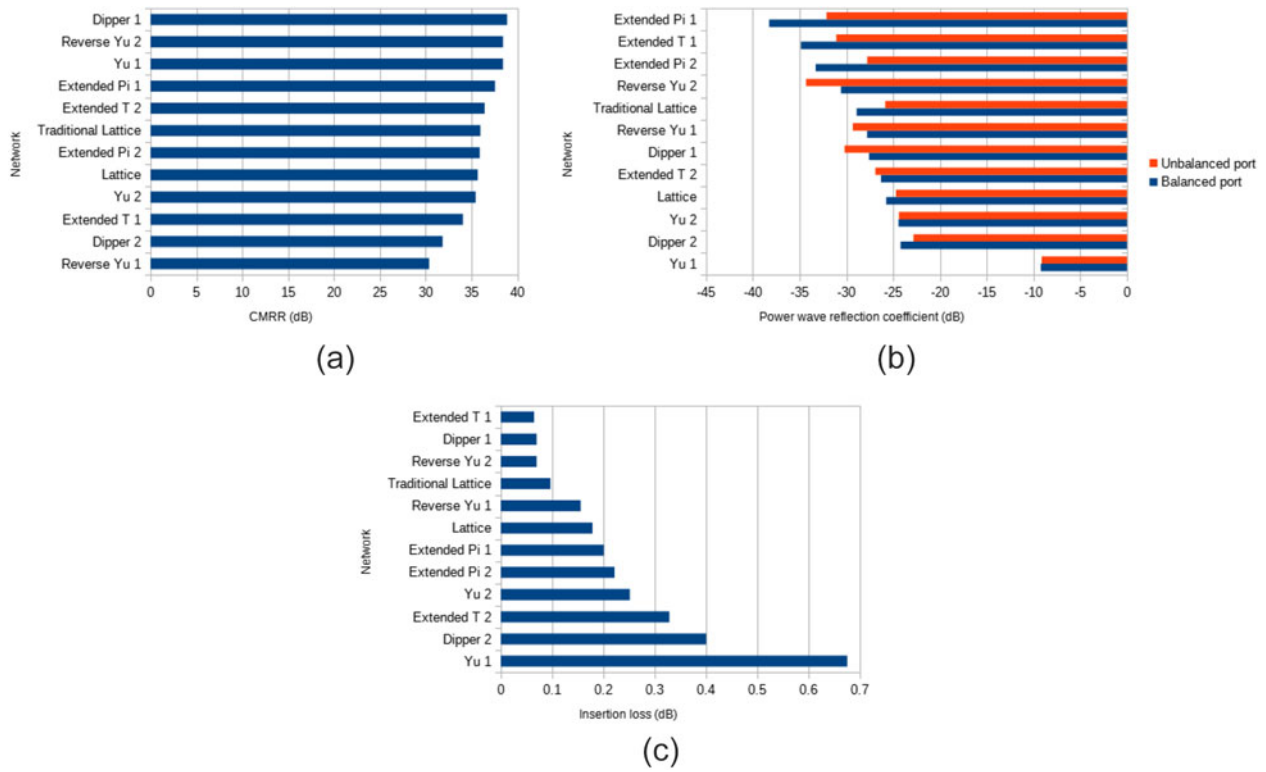


Figure A1. (a) CMRR, (b) power wave reflection coefficients, and (c) insertion loss for each network for the first test case at the design frequency.

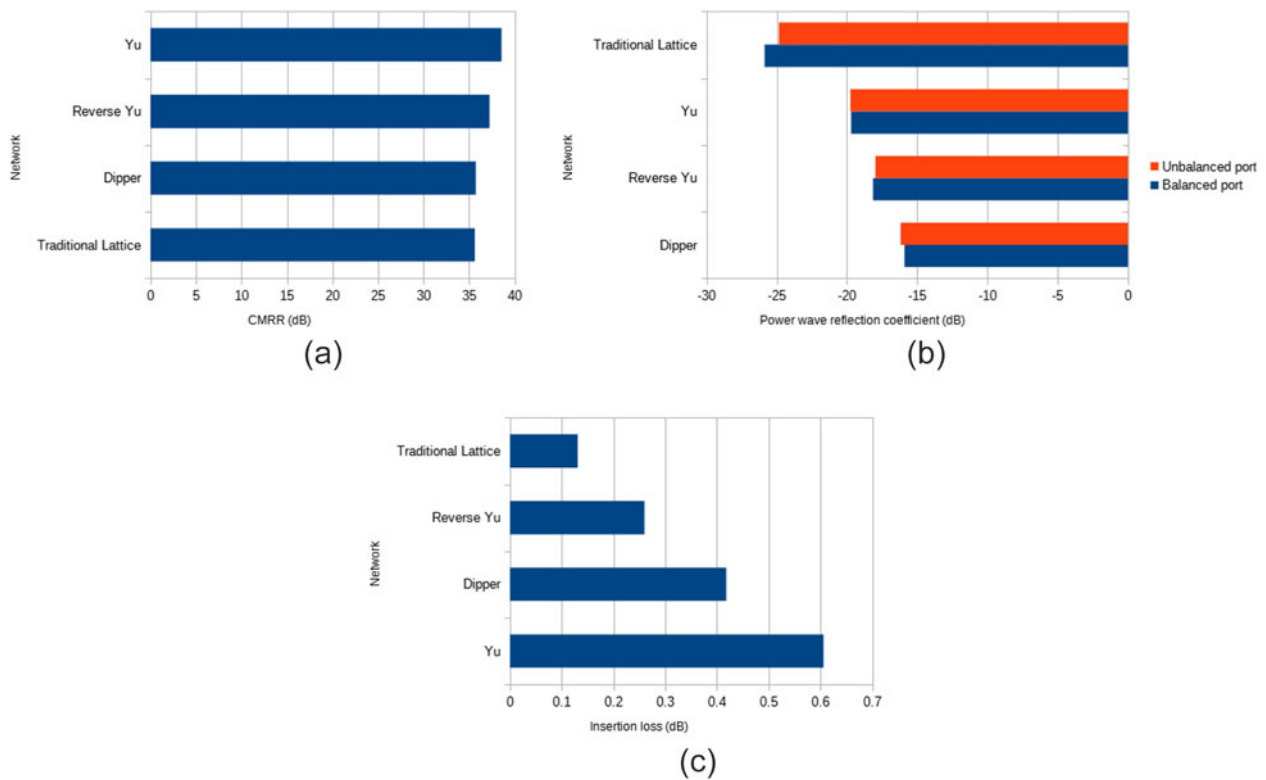


Figure A2. (a) CMRR, (b) power wave reflection coefficients, and (c) insertion loss for each network for the second test case at the design frequency.

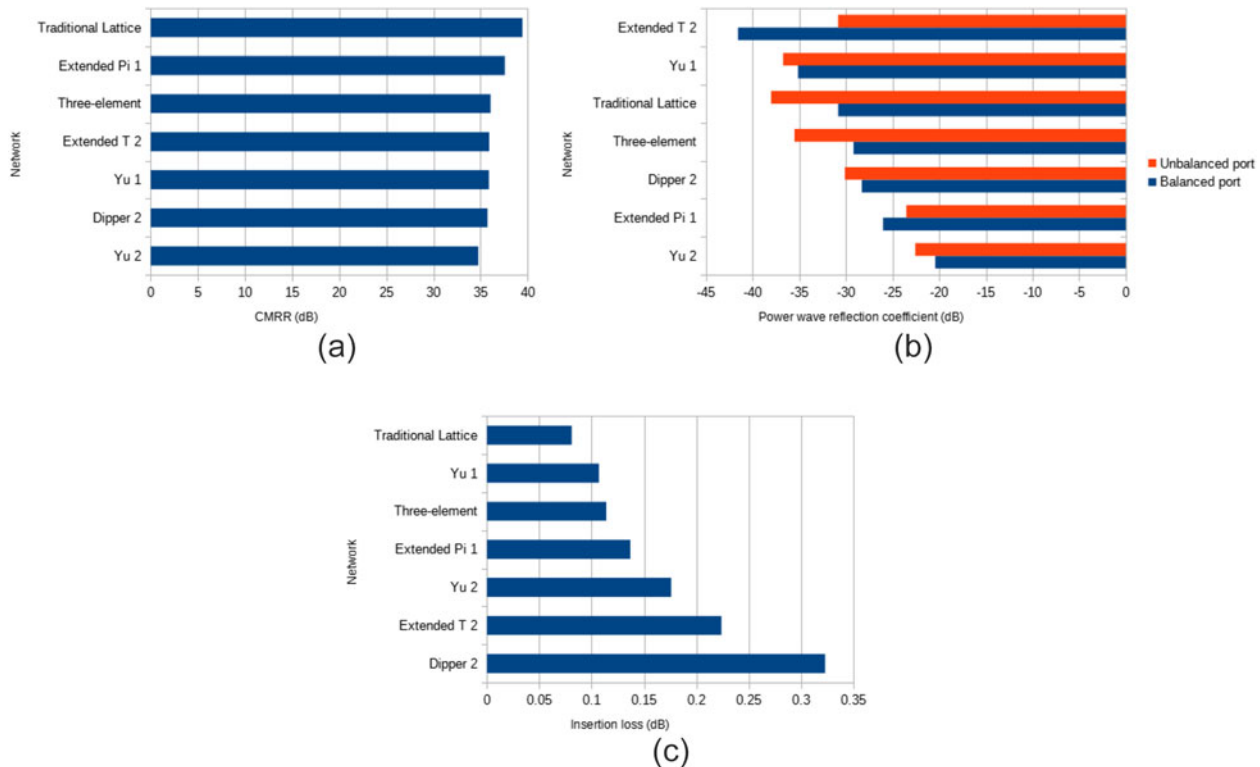


Figure A3. (a) CMRR, (b) power wave reflection coefficients, and (c) insertion loss for each network for the third test case at the design frequency.

Appendix B. Experimental data processing

Before fabrication, the example balun networks were verified with co-simulations in ADS Momentum. Series RLC components were used to model capacitors [16]. Touchstone models were also used to model inductors [15]. Negative length microstrip lines were used to de-embed the microstrip lines connecting PCB ports to SubMiniature version A (SMA) connectors. Capacitance values were altered in the range of the manufacturer tolerances to account for component tolerance effects. The schematics use 1:1 transformers to ensure that the ground pins are not artificially shorted together outside the EM simulation.

ADS simulations were used to perform de-embedding on the combined three-port S-parameters for the network measurements such that the CMRRs and differential two-port parameters could be found. Two layers of de-embedding are used in these manipulations to de-embed transmission line effects due to the SMA connectors and due to the microstrip lines. The simulations for the differential two-port parameters used $50\ \Omega$ reference impedances to allow for the parameters to be exported as Touchstone files. A Jupyter notebook was then used to calculate the power wave reflection coefficients and insertion loss from the Touchstone export for each network using scikit-rf [11, 17]. These results were determined after renormalizing the three-port parameters for reference impedances of Z_U , $Z_B/2$, and $Z_B/2$ at ports 1, 2, and 3, respectively.



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