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Exploring the physical limits of transistor scaling using STEM

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The smallest features on transistors used in computer circuits today have approached atomic dimensions: the SiO_2 gate oxides are between 5 and 8 silicon atoms thick and the concentration of dopant atoms has increased to the point that electrically inactive dopant clusters as small as a few atoms have become common enough to affect device performance. We have used atomic-resolution scanning transmission electron microscope with single atom sensitivity to identify the size, structure and distribution of clusters responsible for the saturation of charge carriers[1] and address the question of how many atoms are needed before the gate oxide loses its bulk properties[2] (fig. 1).

Fig. 2 shows that the dopant concentration cannot be increased without limit, and in fact reaches a maximum at a point below that need for the 2008 generation of devices. Whether this limitation is intrinsic or can be overcome by clever processing is a matter of great concern. From annular dark field STEM images of single Sb dopant atoms buried inside a silicon crystal, we have been able to identify clusters containing only 2 Sb atoms as the defect responsible for the electrical behavior shown in fig. 2[1]. Such clusters are a consequence of a random dopant distribution.

As to the scaling limit for SiO_2 gate oxides, from the analysis of O-K edge EELS fine structure recorded across gate oxides of ever-diminishing thicknesses, we find that the electrical transition region from Si to SiO_2 occurs over a region that is 0.3-0.4 nm wide, even when the structural transition is atomically abrupt. This puts a fundamental limit of 0.7 nm on the oxide thickness in order for the bulk SiO_2 properties to be achieved (fig 1)[2, 3], and provides a challenge for the design of replacement gate dielectrics, many of which contain a few monolayers of SiO_2.

In the search for replacements for the SiO_2 gate oxide, one outstanding problem has been in reducing the fixed charge density in the gate stack, where a flatband or threshhold voltage shift of even a few tens of millivolts impacts device performance. Fig. 3 shows a HfO_2/SiO_2 replacement gate dielectric stack before and after annealing. O-K edge EELS from such films is shown in fig. 4. O-K spectra from monoclinic crystallites exhibit a more strongly pronounced crystal-field splitting with increasing anneal temperature up to 1000ºC, consistent with a decrease in point defects. Concomitantly, electrical measurements of the same structures show a correlated reduction of fixed charge from 5.2 10^{11} e/cm^2 prior to annealing, to 2.9 10^{11} e/cm^2 at 600 ºC to -0.6 10^{11}e/cm^2 at 800ºC. This suggests that with proper control of vacancies and other point defects, the fixed charge might be reduced to a level competitive with the best SiO_2 gate oxides (10^{10} e/cm^2 or better).

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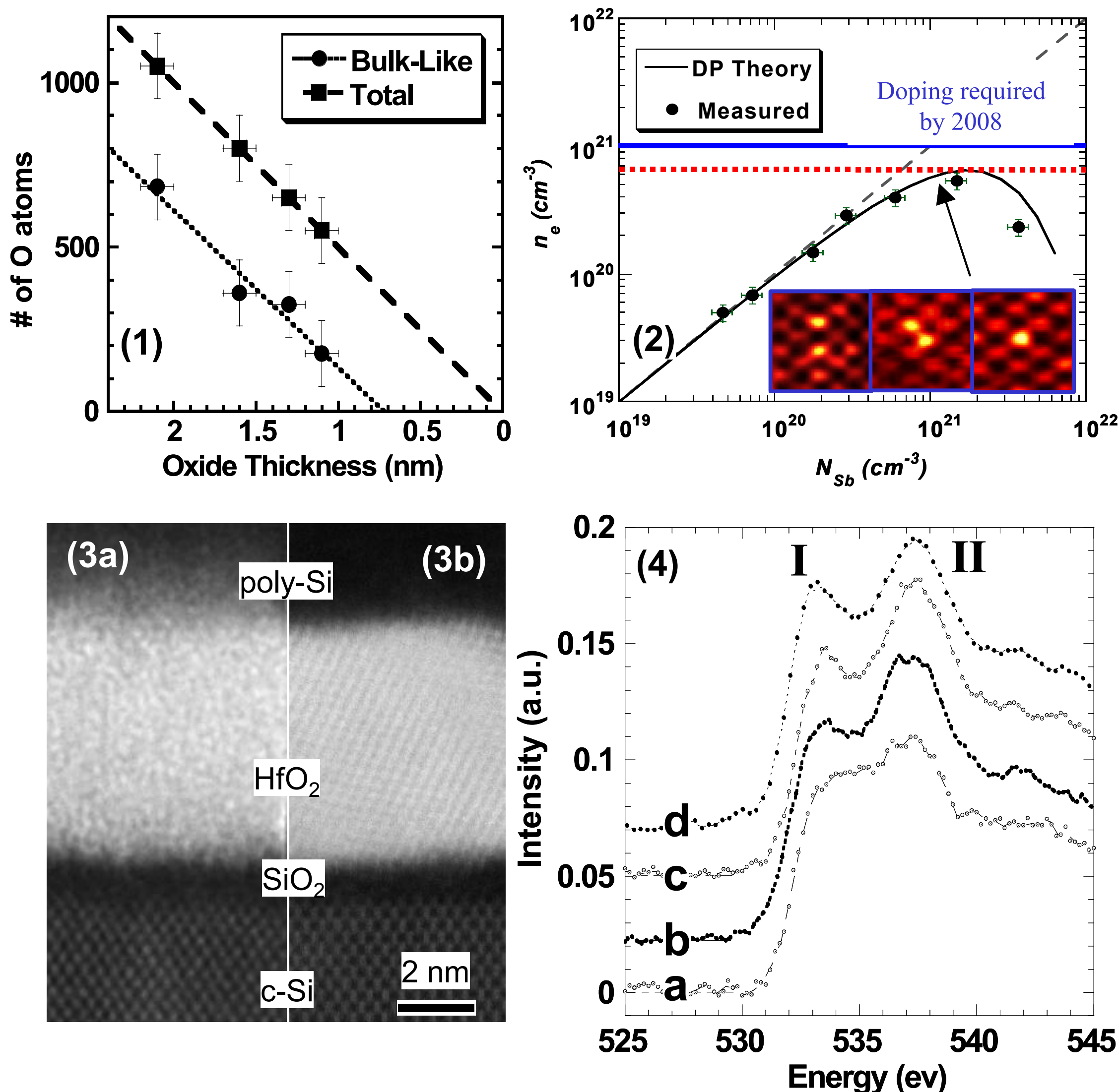

FIG 1. The number of O atoms with bulk-like and interfacial bonding arrangements (as measure by O-K Edge EELS) plotted as a function of gate oxide thickness. There is no more bulk-like silicon dioxide when the gate oxide is less than 0.7 nm thick. Only the interface states remain[2, 3].

FIG 2. Density of free carriers (n_e) as a function of Sb dopant concentration (n_{Sb})[4]. The peak carrier concentration (…) still falls below the 2008 semiconductor roadmap requirements[5]. Inset: ADF STEM images of the Sb dopant clusters responsible for the decrease in carrier activation.

FIG 3. ADF images of HfO_2 gate dielectric on SiO_2 (a) before, showing a quasi-amorphous HfO_2 layer and (b) after annealing in O_2 for 30 sec at 600 °C, showing a crystallized layer.

FIG 4. O-K edge fine structure in HfO_2 films after different annealing regimes: (a) unannealed, (b) 600 C for 30s, (c) 850 C, (d) 1000 C. Spectra (b)-(d) were recorded from single grains of the monoclinic phase in zone-axis orientation. (a) was amorphous. There is a systematic sharpening and intensity increase of the peak labeled I, with respect to peak II. This is correlated with a reduction in the number of electrically measured defect charges.

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