

A Chip Scale Atomic Clock Driven Receiver for Multi-Constellation GNSS

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This paper presents the design and implementation of a Chip Scale Atomic Clock (CSAC) driven dual-channel Digitally Configurable Receiver (DCR) for Global Navigation Satellite Systems (GNSS). The receiver is intended to be used for research applications such as; multipath mitigation, scintillation assessment, advanced satellite clock and spatial frame transformation modelling, Precise Point Positioning (PPP) as well as rapid development and assessment of novel circuits and systems for GNSS receivers. A novel sub-Nyquist sampling (subsampling) receiver architecture incorporating dual-band microstrip RF filters is employed in order to minimize the complexity of the multi-frequency Radio Frequency (RF) front-end. Moreover, the digital receiver incorporates a novel and complexity-reduced Fast Fourier Transform (FFT) core for signal acquisition as well as COordinate Rotation DIgital Computer (CORDIC) cores for the code/carrier discriminators in order to minimize the resource allocation on the FPGA. The receiver also provides easy access to enable adjustment of its internal parameters such as; RF gain, position update rate, tracking channel correlator spacing and code/carrier loop noise bandwidth. Correlator outputs, code/carrier error, Carrier-to-Noise Ratio (C/N_0), navigation and RINEX data are provided to the end-user in real-time. This paper collectively highlights and reports on the implementation, test and validation of the novel techniques, elements and approaches in both the RF and digital part of the DCR that comprise the multi-constellation receiver.

KEY WORDS

1. Receiver. 2. GNSS. 3. Multi-constellation. 4. Atomic Clock.

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1. INTRODUCTION. The new Global Navigation Satellite System (GNSS) signals are designed to provide better positioning accuracy, robustness against the effects of multipath and interference, and ionospheric delay estimation capabilities that would enable minimization of one of the biggest error sources in radio navigation (Akos et al., 2003; Hoult et al., 2008). Evidently, next generation GNSS receivers should be able to tune in to the band of interest to comply with the modulation

standard as and when desired to benefit from the capabilities outlined above. The two challenges faced in the realization of a multi-constellation GNSS receiver are the delivery of the RF signal to the baseband signal processors with a minimal number of RF/analogue components whilst maintaining a high C/N_0 and real-time signal tracking with low-power and cost (Ucar et al., 2012). These challenges are difficult to meet in a receiver tailor-made for research applications such as multipath mitigation (Groves et al., 2010), scintillation assessment (Yang et al., 2011), advanced satellite clock modelling (Davis et al., 2012), spatial frame transformation modelling (Bahrami and Ziebart, 2011) and Precise Point Positioning (PPP) (Jokinen et al., 2012) where a high precision positioning solution with a fast position update rate is essential.

In this paper, we present the design and implementation of a multi-constellation receiver, simply called the Digitally Configurable Receiver (DCR). The DCR, which is also known as a Software Defined Radio (SDR) in the literature, provides an efficient solution to deal with the challenges outlined above. An overview of the DCR is provided in Figure 1. The RF front-end of the DCR is fabricated on a single board incorporating two RF channels that are capable of delivering civilian GPS L1/L2/L5, GLONASS L1/L2 (referred to as G1/G2) and Galileo E1/E5 signals from Left and Right-Hand Circularly Polarized (LHCP/RHCP) antennae to the Analogue-to-Digital Converter (ADC). Three daughter clock boards were fabricated. These facilitate the connection of either a Caesium (Cs) atomic clock (CSAC) (Symmetricom, 2011) or a miniature Rubidium (Rb) atomic clock (Symmetricom, 2012) or an Oven-Controlled crystal Oscillator (OCXO) (Valpey Fisher, 2012) to the RF board in order to generate the master clock that drives the ADC as well as the tracking channels on the Field Programmable Gate Array (FPGA). The CSAC has superior stability that exhibits comparable power consumption to that of an OCXO. The ADC simultaneously down-converts and digitizes the incoming RF signals to an Intermediate Frequency (IF) using the sub-Nyquist sampling (subsampling) approach (Vaughan et al., 1991). The 4-bit digital IF signal from each RF channel is captured by a Virtex-5 FPGA board that carries out the Digital Signal Processing (DSP) in conjunction with a Linux workstation. This setup provides two synchronized receivers that are integrated into one piece of hardware with an external clock. The rest of the paper is organized as follows: Section 2 introduces the fabricated RF front-end; Section 3 describes the digital receiver incorporating a Virtex-5 FPGA and a Linux workstation; Section 4 presents a performance evaluation of the receiver using real-time tracking experiments and, finally, Section 5 contains the concluding remarks.

2. RF FRONT-END. The system-level architecture of the dual-channel RF front-end is given in Figure 2. The RF front-end incorporates two RF channels having identical circuit components within the constraints of component matching. The RF chain applies 90 to 120 dB amplification on the received signals, which can be controlled from the user interface on the Linux workstation with the help of a 10-bit Digital-to-Analogue Converter (DAC) and the FPGA. Intentional aliasing of the RF signal via subsampling eliminates the need for RF mixers and IF-stage analogue filters, thereby providing a low-cost, reduced complexity solution for the front-end. Furthermore, the receiver employs a novel dual-band microstrip filter

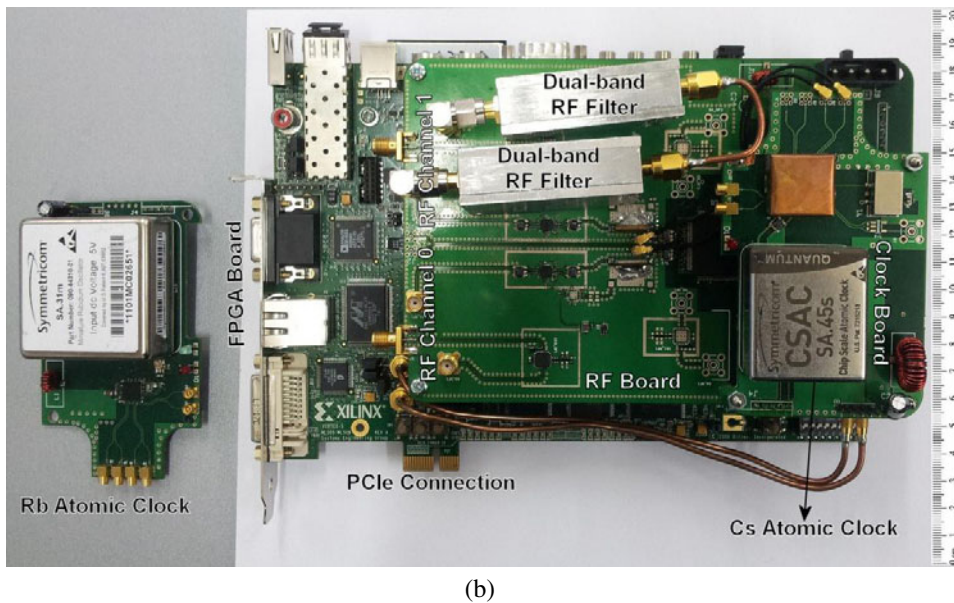
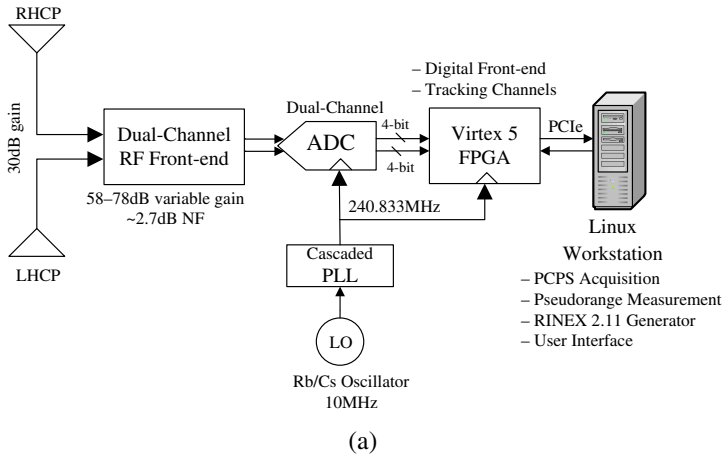


Figure 1. (a) Block diagram of the receiver, (b) Realization of the receiver with the the Cs atomic clock on-board. (The dismantled Rb atomic clock board is depicted on the left)

(Adane et al., 2011; Tugrul et al., 2011) at RF, which gives a simple solution compared to employing an RF filter per GNSS band (Akos et al., 2003).

2.1. *RF Filters.* Down-converting an RF signal to an IF by employing subsampling results in a poorer Signal-to-Noise Ratio (SNR) compared with that from performing a down-conversion with an RF mixer (Pekau and Haslett, 2006). In order to minimize the out-of-band noise at the output of the ADC, subsampling receivers impose stringent requirements on the selectivity of the Anti-Aliasing (AA) filters preceding A/D conversion (Ucar et al., 2008). An opportunity for a reduced complexity solution emerges when the GNSS spectrum, as illustrated in Figure 3(a),

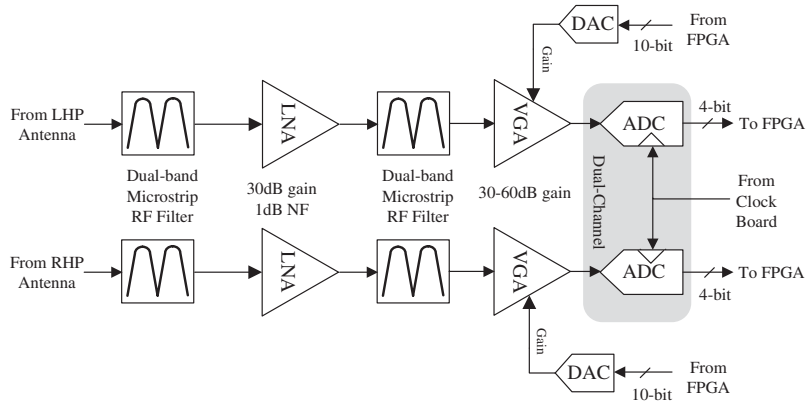
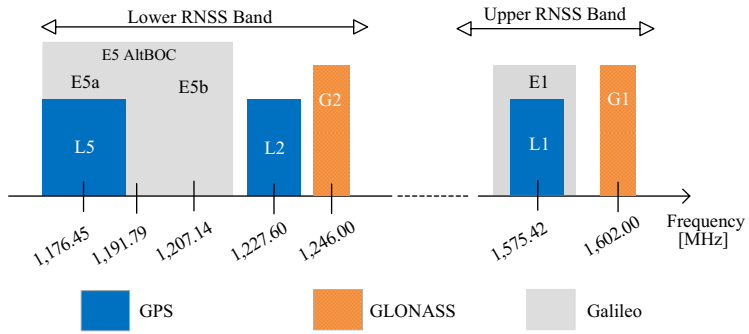
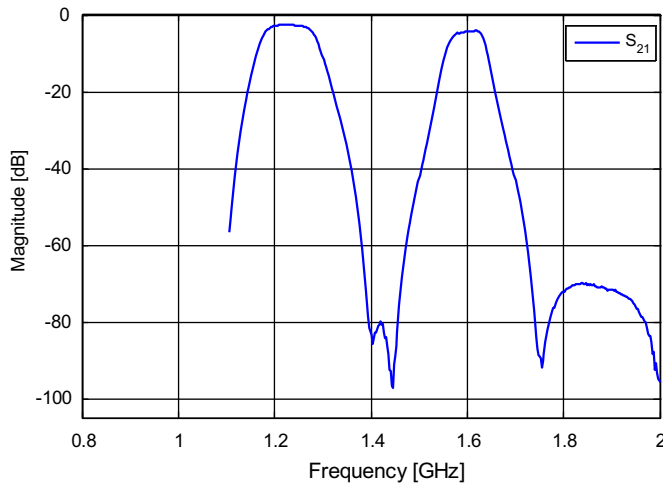


Figure 2. Block diagram of the subsampling RF front-end.



(a)



(b)

Figure 3. (a) GNSS frequency plan for the signals of interest, (b) Measured frequency response of the cascaded novel dual-band microstrip RF filter.

Table 1. Reference oscillators used for master clock generation.

Clock	Frequency	Phase Noise @1 KHz	Allan Deviation @1 s	Power
Caesium SA.45 s CSAC	10 MHz	< -128 dBc/Hz	1.5×10^{-10}	< 120 mW
Rubidium SA.31 m	10 MHz	< -130 dBc/Hz	5×10^{-11}	~ 5 W
VFOV400 OCXO	10 MHz	-155 dBc/Hz	4.4×10^{-6}	< 120 mW

is examined. A dual-band RF filter can be utilized as an AA filter to select the signals of interest within the lower and upper Radio Navigation Satellite Systems (RNSS) band. Such a filter was realized based on half-wavelength octagonal open-loop resonators (Tugrul et al., 2011). The dimensions of each filter, excluding the aluminium shielding box, are 2.19 cm × 2.07 cm and they deliver a clear and sharp carving of the frequency bands out of the total spectrum, as illustrated in Figure 3(b). The insertion loss for the lower and upper pass bands are 2.5 dB and 2.7 dB, respectively. The dual-band filter is the critical component that enables simultaneous processing of multiple GNSS signals as it is made to span the entire GNSS spectrum.

2.2. Clock Generation. The master clock is generated on a separate mezzanine board that can be mounted on the main RF board. This approach enables evaluation of the performance of different types of oscillators with respect to phase noise and stability. The presence of atomic clocks on board provides highly stable reference oscillators, with comparable performance to the atomic clocks on board the satellites, with low frequency stability for superior receiver performance. Atomic clocks are employed as the receiver is intended for high-end research and development applications in investigating the performance of new algorithms as well as work relating to orbits and spatial frame transformation modelling. Table 1 gives the characteristics of the three different oscillators employed for the master clock generation. The Cs/Rb atomic clocks employed as clock reference have superior stability as can be observed; however, they have larger phase noise than a crystal oscillator. The sampling jitter is one of the most critical parameters in subsampling receivers. The sampling jitter increases the thermal noise level at the output of the ADC, which results in reduced receiver sensitivity. To compensate for the relatively large phase noise, the master clock is generated using a precision clock conditioner that provides “jitter cleaning” by cascading two Phase Locked Loops (PLL) (Texas Instruments, 2011). The first PLL, in which the oscillator is the clock reference, is used with a relatively narrow loop bandwidth to retain the accuracy of the clock frequency. The low phase noise provided by the first PLL enables the use of a wider loop bandwidth for the second PLL. The phase noise at the output is dominated by the first PLL at low offset frequencies and the second PLL at high offset frequencies. The measured Root Mean Square (RMS) jitter of the generated 250 MHz clock, when the Cs CSAC is used, is as low as 150 fs. Atomic clocks are connected to the FPGA board via their built in RS-232 interfaces. Therefore, the Linux workstation may be used to control and calibrate the atomic clocks as well as to receive status updates from the clocks. A temperature sensor is also placed on the clock board to provide real-time temperature monitoring in order to observe and compensate for long-term temperature effects.

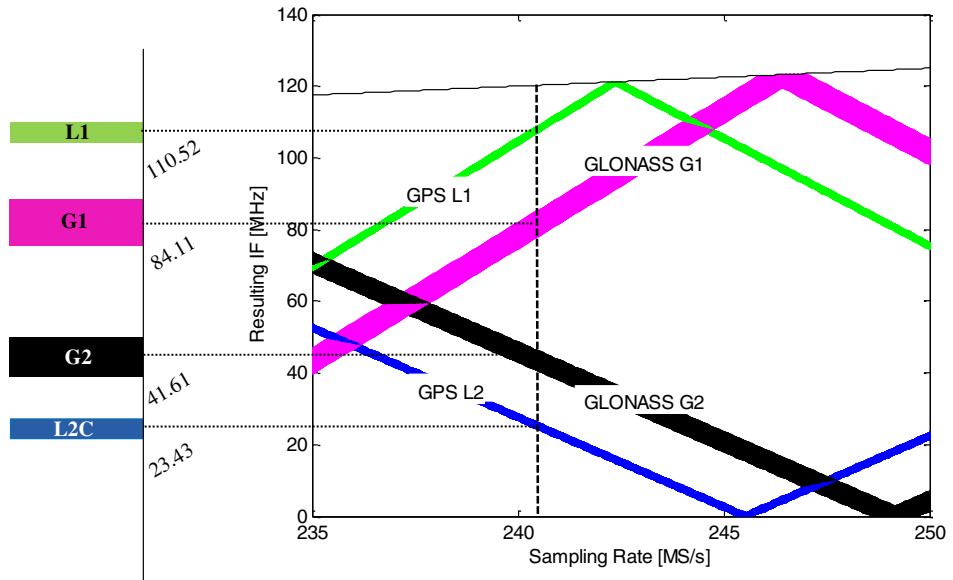


Figure 4. Ladder diagram showing the minimum sampling rate to avoid destructive aliasing for simultaneous down-conversion of GPS L1/L2C and GLONASS G1/G2.

2.3. *Analogue-To-Digital Conversion.* Subsampling achieves frequency translation via intentional aliasing of the desired RF signal to an IF without the need for RF mixers. In a subsampling receiver, the sampling rate of the ADC determines the location of the down-converted digital signal within the sampled spectrum. When signals from multiple frequencies are simultaneously subsampled, the sampling rate must be chosen carefully to avoid spectral overlap between signal aliases. In this case, the alias ladder diagram (Akos, 1997) can be used to determine the set of suitable sampling rates.

The ladder diagram to find the minimum sampling rate for simultaneously down-converting GPS L1/L2C and GLONASS G1/G2 is given at Figure 4. The resulting centre frequency of a particular signal after subsampling is the intersection of the dashed sampling rate line at 240.833 MHz with the strip representing the signal. Since GNSS signals are spread-spectrum, the dynamic range requirement need not be high. Nevertheless, the receiver must accommodate for the maximum expected magnitude of interference (Kaplan and Hegarty, 2006). Signals are still below the thermal noise floor at the input of the ADC, therefore, the amplification provided by the RF front-end raises the thermal noise floor level to the ADC's full-scale range. The Variable Gain Amplifier (VGA) on board ensures that the magnitude of any interference does not exceed the thermal noise floor. The ADC resolution per RF channel is 8-bits, although 4-bits are currently used for digital processing. The ADC-FPGA interface utilizes Low-Voltage Differential Signalling (LVDS) at 120.416 MHz since the ADC is time-interleaved by a factor of two.

3. **DIGITAL SIGNAL PROCESSOR.** The 4-bit digital IF signal transmitted from each RF channel is captured by the Virtex-5 FPGA board, ML506, that

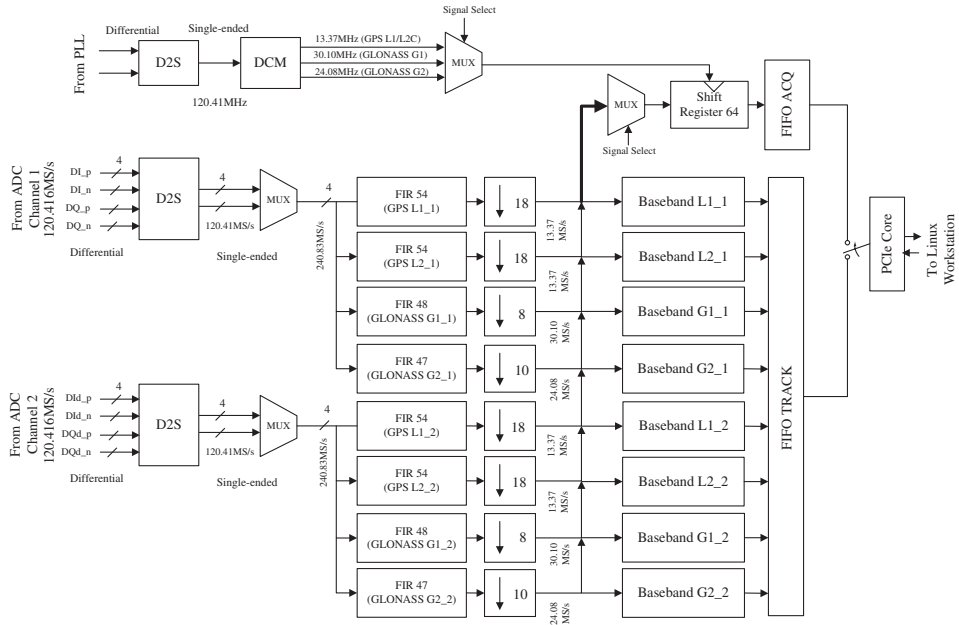


Figure 5. Hardware architecture of the digital receiver.

runs the rest of the receiver’s tasks in conjunction with the Linux workstation. The overall hardware architecture of the digital receiver that is mapped on to the FPGA chip is shown in Figure 5. A hardware/software co-design approach is adopted in the digital receiver in order to provide an easy access to control the receiver parameters from the PC and be able to use the workstation for some of the receiver tasks, such as; Parallel Code Phase Search (PCPS) acquisition, pseudo-range measurement and Receiver INdependent EXchange format (RINEX) file generation. The FPGA board is connected to the Linux workstation via a high-speed Peripheral Component Interconnect express (PCIe) 2-0 interface having a throughput rate of 500 MB/s. The tracking channels are implemented on the FPGA and are driven by the master clock that also drives the ADC. This arrangement provides two highly synchronous receivers and guarantees superior stability when the master clock is generated using the atomic clocks.

3.1. *Digital Front-End.* The sampled signal spectrum at the output of the ADC is illustrated on the left-hand side of Figure 4(a), where the signals of interest for baseband processing, L1, L2C, G1, and G2, are centred at 110.52 MHz, 23.34 MHz, 84.23 MHz, 41.53 MHz, respectively. The digital front-end is responsible for delivering the signals from the ADC to the correlators with minimum aliasing and as low a sampling rate as possible. There is a trade-off between the resulting signal distortion at the output of the digital front-end and power-consumption in the baseband processors. The digital front-end consists of 8 Finite Impulse Response (FIR) filters each followed by a down-sampler as there are 2 RF channels and 4 signals down-converted by the ADC per RF channel. FIR filters are implemented using the Time Delay and Accumulate (TDA) structure to provide a low latency and to enable the efficient use of DSP slices within the FPGA chip. The co-efficient word-length deployed is 16-bits and the filter order for L1, L2C, G1, and G2 are

Table 2. Frequency Plan for the Digital Receiver.

Signal	RF [GHz]	Initial IF [MHz]	Final IF [MHz]	Final Sampling Rate [MS/s]
GPS L1	1.57542	110.52	3.37896	13.37965
GPS L2C	1.22760	23.34	3.32800	13.37965
GLONASS G1	1.60171	84.23	6.19522	30.10421
GLONASS G2	1.24578	41.53	6.55419	24.08337

54, 54, 48, and 47, respectively. Down-sampling at the output of the FIR filters aliases the signals to a very low IF, as given in Table 2 as the final IF. The output of the filters is truncated back to 4-bits after down-sampling, which is followed by signal acquisition.

3.2. Acquisition. The serial-search acquisition technique, which calculates correlations in the time-domain, is time consuming and not suitable for a receiver processing the next-generation GNSS signals, especially since the spreading codes for the new signals are longer. The frequency-domain Parallel Code Phase Search (PCPS) technique parallels the search for the code phase by calculating the correlation in the frequency domain (Lin and Tsui, 1998). The search space is cut down to code phase combinations at the expense of increased hardware complexity – in our case FPGA resources. The hardware complexity behind the PCPS acquisition comes from the forward and inverse Fourier transformations. The DCR offers two solutions for this problem, one of which is novel.

The first solution is to start the FPGA in data capture mode when the receiver is first initialized. In data capture mode, the 4-bit digital IF data from both RF boards are transmitted to the Linux workstation via the PCIe link in order to perform PCPS acquisition sequentially on the PC. The PCPS acquisition performed on the PC is implemented in C/C++ using an open source FFT library (Frigo and Johnson, 1998). It takes 7 to 30 s for cold start and 3 to 12 s for warm start acquisition per signal depending on the sampling rate. Once all signals are acquired, the FPGA switches to real-time tracking mode. The drawback of this approach is the interruption of signal tracking during the acquisition of new satellites.

The second solution tackles this problem by implementing the PCPS acquisition on the FPGA using an efficient implementation of FFT, optimized for GNSS signal acquisition (Bardak et al., 2011). The novel FFT algorithm reduces the computational complexity of the high precision FFT, that requires many bits to compute the spectrum, to one that delivers almost the same spectral result but with far fewer bits, resulting in a lower complexity hardware solution. The novel FFT implementation is based on the radix-2 Decimation in Frequency (DiF) structure (Proakis and Manolakis, 2007). The basic idea is to maximize the sensitivity of GNSS signal acquisition whilst minimizing the computational load through an extensive noise analysis and optimization of word-lengths of twiddle factors and partial products of the FFT calculation. The word-length constraints are determined according to the IF of the signal and the Signal-to-Quantization Noise Ratio (SQNR) of the FFT output. The word-length constraints are modified using a weighted absolute error checking approach, based on the least square residual approximation. The approximation algorithm sets the results obtained from the PCPS acquisition with the full precision

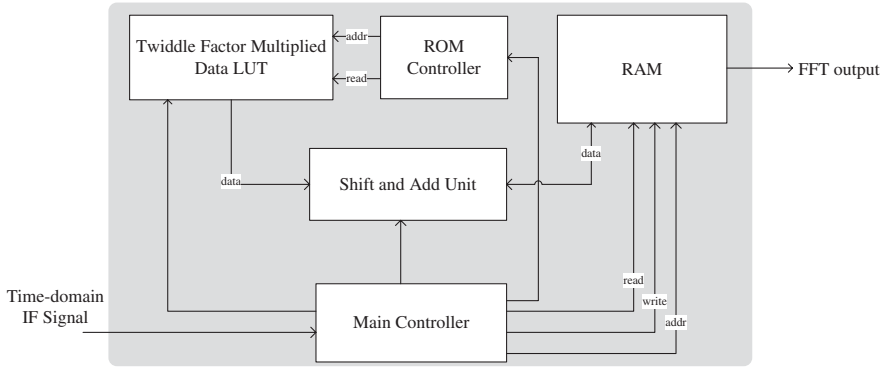


Figure 6. Hardware architecture of the novel FFT implementation for PCPS acquisition.

FFT as the target and modifies the world-length constraints at every stage of the novel reduced-complexity FFT. The hardware architecture, as shown in Figure 6, relies on deploying flexible and configurable algorithms for the multiplication of every node within the FFT unit and saves the results into memory using a reduced number of bits. The hardware architecture of the novel FFT unit incorporates; a shift and add unit, a main controller and memory/Look-up Table (LUT) units.

The FPGA version of PCPS acquisition block using the novel FFT implementation delivers almost identical results when compared to floating point C/C++ implementation. The FPGA-based PCPS acquisition using the novel FFT architecture is currently being integrated into the DCR.

3.3. *Tracking.* Tracking channels, as illustrated in Figure 7(a), are implemented on the FPGA chip to enable real-time signal tracking. The number of tracking channels per baseband processor can easily be reconfigured in order to efficiently use the resources on the FPGA. Baseband processors run at a much higher clock rate than the final sampling rates as shown in Table 2. This is because FPGA processing resources are limited, and a multi-constellation and dual RF-channel receiver requires a large number of tracking channels. This makes the time-multiplexed processing approach crucial in making the design small enough to fit onto the Virtex-5 FPGA. After the initialisation values have been loaded from the acquisition stage, the tracking channels produce Early (E)/Prompt (P)/ Late (L) correlations which are sent to both the PC for post-processing and also to the FPGA discriminator/loop filter unit. The initial Doppler shift calculated within the acquisition block with an accuracy of 10 to 15 Hz on the carrier is used to initialize the code and carrier Numerically Controlled Oscillators (NCOs) on the FPGA. The 4-bit \times 4-bit carrier wipe-off is implemented with LUTs. As mentioned above, after calculating time-domain Early (E)/Prompt (P)/ Late (L) correlations for the duration of code period, the outputs of each Accumulate & Dump unit are sent to the discriminator/loop filter unit.

A single discriminator/loop filter unit is implemented per baseband processor as arithmetic operations required for the code/carrier discriminators take a significant amount of resources on the FPGA. It takes 300 ns for the discriminators to compute the updated code/carrier frequencies per tracking channel and the throughput is one channel every 138 ns. Therefore, time-multiplexing can be facilitated within a baseband processor to share the discriminator/loop unit amongst the tracking

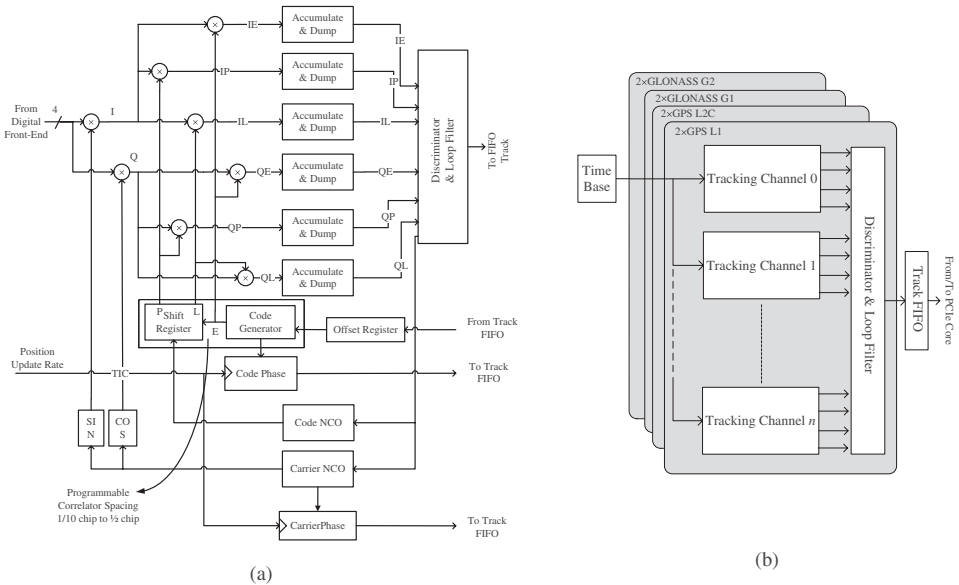


Figure 7. Hardware architecture of: (a) A single tracking channel with the word-lengths optimized for the GPS L1 signal and (b) A combination of $n+1$ tracking channels within the baseband processor.

channels, as illustrated in Figure 7(b). The code discriminator (Kaplan and Hegarty, 2006) requires the magnitudes of complex numbers to be calculated, this is achieved using a custom COordinate Rotation DIgital Computer (CORDIC) core. The remaining code discriminator operations are carried out using the available DSP slices with the intention of minimizing the computation time. The hardware architecture of the code discriminator/loop filter is depicted in Figure 8(a). The maximum deviation in the code error is 8×10^{-6} chips when compared with C/C++ floating-point implementation of the code discriminator. The carrier discriminator, on the other hand, requires the arctangent operator $atan(y, x)$. The hardware architecture of the carrier discriminator is illustrated in Figure 8(b). The maximum deviation of the carrier error is 4×10^{-10} radians when compared with the C/C++ floating-point implementation, as illustrated in Figure 9. The code and carrier errors are filtered by a first order programmable Infinite Impulse Response (IIR) filter having two coefficients (C_1 , C_2) to calculate updated code/carrier frequencies. Once the updated code/carrier frequencies are transmitted to the code/carrier NCOs, the tracking loop is complete. The coefficients of the filter are based on the loop noise bandwidth, damping ratio and gain. The user interface running on the Linux workstation can be employed to modify the E/P/L correlator spacing, the code/carrier loop filter bandwidth/damping ratio/gain and position update rate on-the-fly as the tracking process is on-going.

3.3. *Position Computation.* Pseudo-range estimation and RINEX data generation for the receiver is done in real-time on the Linux workstation with applications written in C/C++. The common reception time approach is adopted for pseudo-range estimation as it is more suitable for use in real-time multi-constellation receivers

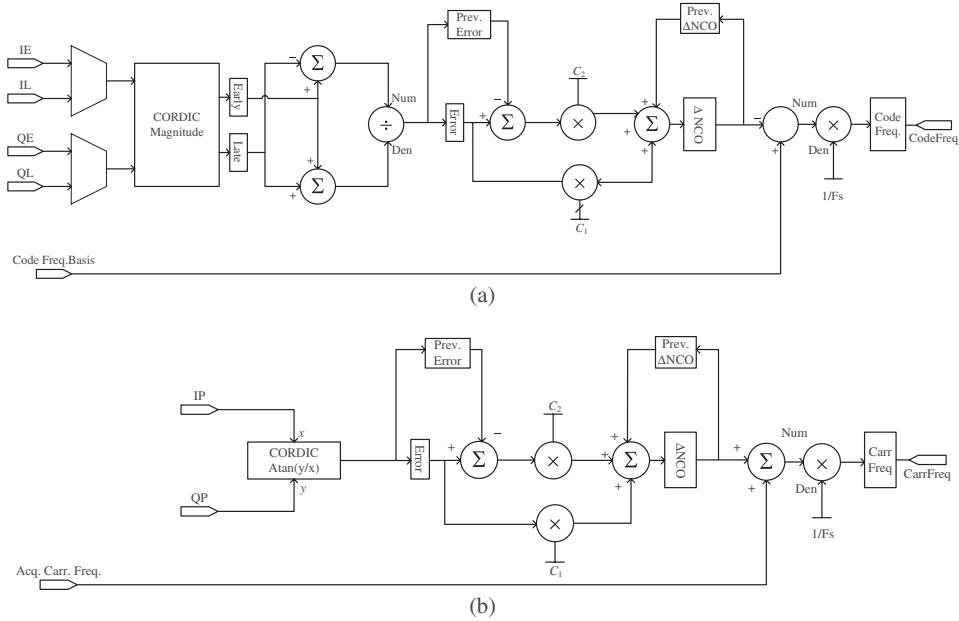


Figure 8. Hardware architecture of: (a) Code discriminator and loop filter and (b) Carrier discriminator and loop filter.

(Rao et al., 2012). The outputs from the FPGA are E/P/L correlator outputs, code/carrier phase and the epoch counter, which is used to store chip and navigation data bit counts. A single position update clock running on the FPGA is latched onto the epoch counter and the code/carrier phase registers in each tracking channel. At each position update, the Time of Emission (ToE) for a particular satellite is calculated using (Misra and Enge, 2011):

$$\begin{aligned}
 \text{ToE[s]} = & \text{Z-count} \times 1.5 \\
 & + \# \text{ of bits transmitted} \times \tau_{\text{ND}} \\
 & + \# \text{ of code epochs} \times \tau_{\text{CODE}} \\
 & + \# \text{ of code chips} / f_{\text{CHIP}} \\
 & + \text{fraction of the code chip} / f_{\text{CHIP}}
 \end{aligned}
 \tag{1}$$

where τ_{ND} is the navigation bit period, τ_{CODE} is the code period, and f_{CHIP} is the chipping rate.

The pseudo-range can then be calculated from:

$$\rho = c \times (\text{ToR} - \text{ToE})
 \tag{2}$$

where ToR is the time of reception and c is the speed of light.

4. EXPERIMENTAL RESULTS. A performance analysis of the DCR was conducted by performing real-time tracking tests with the experimental set-up shown in Figure 10. The Cs SA.45s' CSAC was utilized as the reference oscillator for the

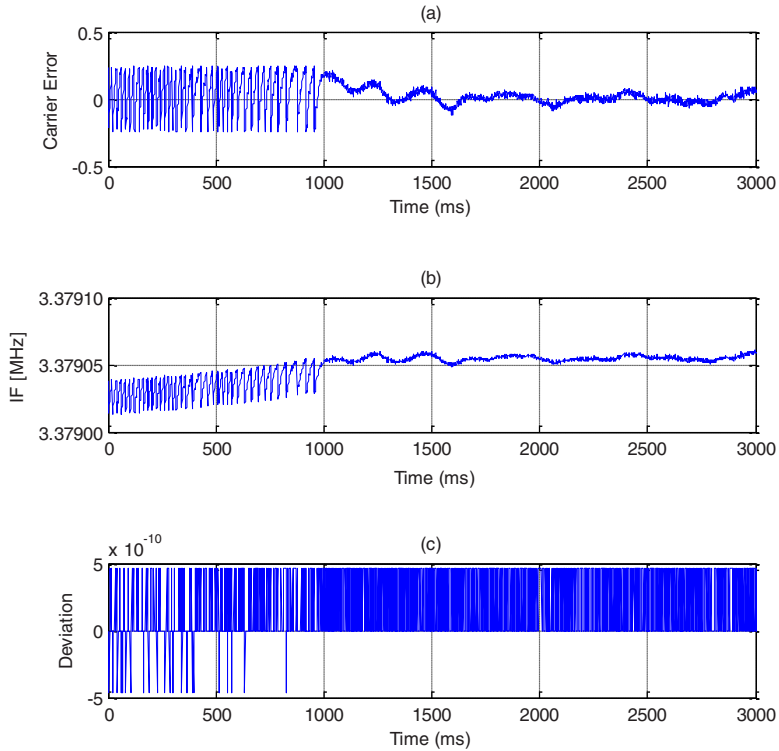


Figure 9. The initialization of the a GPS L1 tracking channel on the FPGA showing: (a) Carrier error, (b) Carrier frequency and (c) The difference in carrier error between the FPGA-based discriminator and floating-point implementation of the discriminator in C/C++.

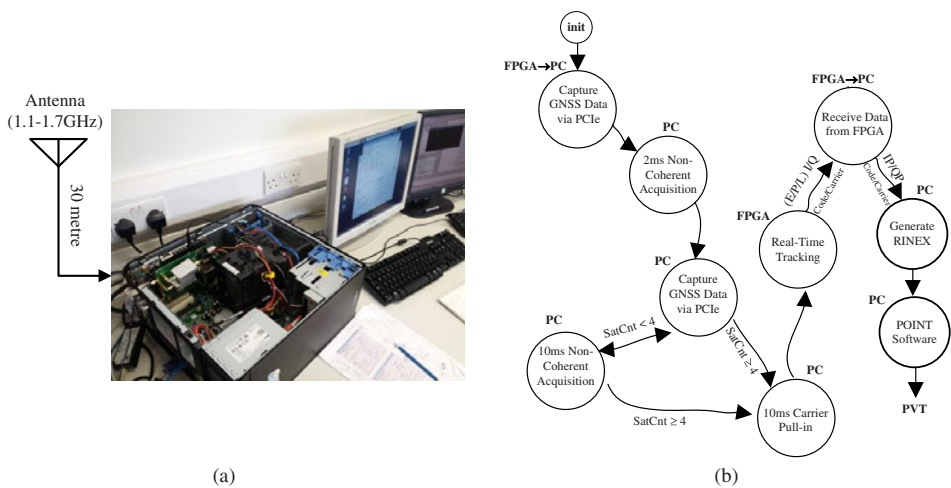


Figure 10. (a) DCR test-bed at Applied DSP and VLSI Research Group, University of Westminster and (b) DCR signal flow-chart for the GPS L1 signal.

Table 3. Average C/N_0 obtained from the real-time tracking experiment (GPS L1).

Satellite	C/N_0 [dB-Hz]	Initial Elevation	Satellite	C/N_0 [dB-Hz]	Initial Elevation
13	47.63	57.1°	05	42.34	28.7°
10	47.01	87.2°	08	40.90	30.0°
02	46.60	49.6°	16	39.98	14.6°
07	44.58	56.4°	29	39.40	9.0°
04	45.17	41.3°	30	37.53	7.3°

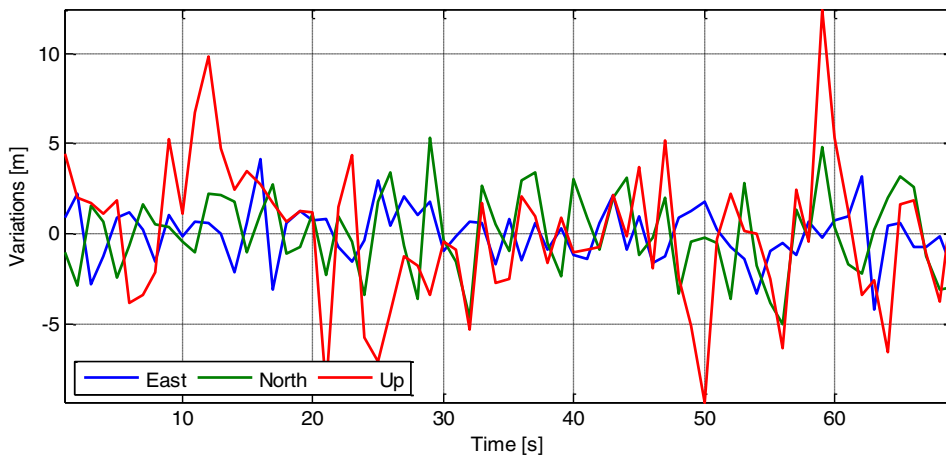


Figure 11. Variation in the positioning solution (Pseudo-range smoothing not applied).

tests. A wideband (1.1 to 1.7 GHz) active antenna placed on the roof of the University of Westminster's Cavendish Campus (Lat. 51.52084, Long. -0.14014) was connected to the DCR test-bed with a 30 m cable. It should be noted that Cavendish Campus is located very close to London's BT telecommunications tower. Therefore, strong RF interference is present in the received signal. Nevertheless, real-time tracking results, as shown in Table 3 for the GPS L1 signal, indicate that the DCR is capable of tracking GNSS signals with a C/N_0 in the range of 47 to 37 dB-Hz. The positioning solution, as shown in Figures 11 and 12, was obtained by feeding the generated RINEX 2.11 file to the POINT software, developed by the University of Nottingham. Pseudorange smoothing using carrier phase observations was not applied to the results shown in these figures. The standard deviation of the position error was measured as 1.525 m (East), 2.302 m (North) and 3.942 m (Up) on the Universal Transverse Mercator (UTM) co-ordinate system, respectively.

5. CONCLUSIONS. A digitally configurable multi-constellation GNSS receiver with the option of driving the tracking channels by Rubidium (Rb)/ Caesium (Cs) atomic clocks was designed and constructed. Experimental results show that the Digitally Configurable Receiver (DCR) is capable of acquiring and tracking all visible satellites with an elevation angle of 5 degrees or more and with an average Carrier-to-Noise Ratio (C/N_0) in the range of 47 to 37 dB-Hz. The RF front-end delivers not only GPS L1/L2C and GLONASS G1/G2 signals, but also GPS L5 and Galileo

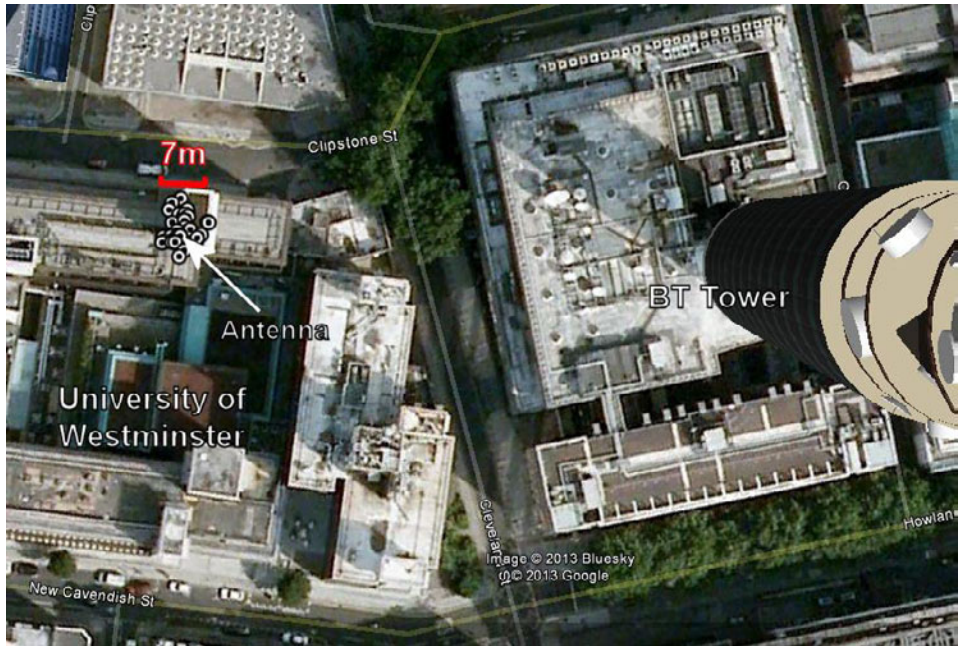


Figure 12. Positioning solution illustrated with Google Earth™ (Black and white circles represent the measurements over time).

E1/E5 signals to the ADC. Therefore, new GNSS signals can be added to the receiver by altering the ADC sampling rate and the FPGA configuration. At present, the position computation for the receiver relies solely on code pseudo-range estimation and can be further improved by using carrier aiding of the code loop and/or pseudo-range smoothing using carrier phase information.

The dual RF channel receiver can be used for research applications, such as multipath mitigation, by connecting the RF channels to left-hand and right-hand polarised antennae and satellite clock modelling by capturing different GNSS signals from each front-end to perform a differential analysis of the clock biases from both systems. The effect of scintillation on signal tracking can also be analysed with the DCR since such analysis requires input spectral diversity with a high update rate and a stable reference clock. The DCR makes it possible to deploy a diverse range of applications involving rapid development, real-time prototyping and assessment of new architectures, circuits and systems for GNSS receivers.

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EADS Astrium, Nottingham Scientific Limited, Leica Geosystems, Ordnance Survey of Great Britain, QinetiQ, STMicroelectronics, Thales Research and Technology UK Limited and the UK Civil Aviation Authority.

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