

Lab-based Nanoscale 3D X-Ray Microscopy for Failure Analysis on Advanced Semiconductors

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3D X-Ray Microscopy (3D XRM) is a key method for analyzing modern semiconductor packages [1]. Due to its non-destructive nature, samples are investigated to find the root cause of dis-functions such as shorts, high resistive opens or electrical opens. Until recently, the main approach for lab-based X-Ray tomography measurements has been based on the principle of geometric magnification (so-called Micro-Computed Tomography or μ -CT) [2]. Here, the sample is placed between a broadband X-Ray source and detector and rotated around its axis while 2D X-Ray projections are acquired. The resulting resolution is then related to the source – detector distance and the spot size of the X-Ray source. 3D XRM extends this capability by using a photon-converting scintillator and optical objectives before the actual detector to achieve high resolution at larger source – detector distances. This procedure, known as resolution at a distance (RaaD [2]) enables the inspection of larger samples and a non-destructive semiconductor package workflow. Typically, the maximum resolution for this kind of method is in the order of 650 – 700 nm with optimum conditions [2]. Continuous transistor node development, increased functionality density and 3D device build up in semiconductor products demands higher resolution X-Ray measurements [3]. Here, 3D XRM is regarded as promising and early publications have proven this to be feasible based on synchrotron results [4, 5]. However, a lab-based method coupled to a repeatable and precise targeted sample preparation workflow is needed to meet the time-critical requirements of the semiconductor industry. A Fresnel Zone Plate (FZP) based solution using quasi-monochromatic X-rays from a laboratory source meets these needs. This XRM architecture allows a significant improvement in optical resolution down to 50 nm and less and opens application opportunities for imaging critical structures within the semiconductor build up, such as Back-end of Line (BEOL, the internal wiring of individual transistor, capacities, etc.) and Chip-Package-Interaction (CPI, the interconnect level between integrated circuit (IC) and substrate or different IC devices).

In order to apply nanoscale 3D XRM on advanced semiconductors, 2 major conditions have to be evaluated and optimized:

1. The use of a monochromatic energy source limits the maximum sample penetration length and therefore requires sample preparation.
2. The X-Ray energy must be selected for use with semiconductor-related materials such as copper, tungsten, silicon and aluminum.

The paper presents a feasibility study that extracts the region of interest by using pico-second laser ablation, figure 1. Using top-down navigation, a 2-step process first separates the ROI area at large from the residual sample. In a second step, the tip of the extracted sample part is further thinned till a 100 μ m thin tip remains. This small tip contains the area that will be investigated by nanoscale 3D XRM while the larger part acts as sample stabilization. The prepared sample is then investigated using different X-Ray sources of 5.4 keV, 8 keV (both Rigaku rotating anode) and 9.2 keV (Excillum metal jet), figure 2. All measurement parameter (exposure time, number of projections, etc.) are identical between measurements and data acquisition was performed on ZEISS Xradia Ultra family microscopes. 3D data

was reconstructed using the filtered back-projection method. The side-by side comparison shows that 5.4 keV shows a good spatial resolution but is unable to fully penetrate the CPI feature that contains a thick copper interconnect. The measurement with 9.2 keV demonstrate contrast within this feature and good spatial resolution, but significant artefacts are seen in the metal layers due to the high absorption in the copper traces. The measurements at 8 keV show the same resolution as those at 5.4 keV and 9.2 keV, but the lower absorption values in the copper traces and the CPI feature result in images with dramatically reduced artefact levels and cleaner images. From this comparison, it was determined that imaging at 8 keV is the optimum X-Ray energy level for these types of semiconductor applications. Further study will optimize imaging conditions and integration with sample preparation workflows to create a useful end-to-end solution for examining local defects in the BEOL and CPI levels of state-of-the-art semiconductor packages.

- [1] C. Schmidt, *et al*, Use of 3D X-Ray Microscopy for BEOL and Advanced Packaging Failure Analysis, International Symposium for Testing and Failure Analysis (ISTFA), (2017).
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- [3] R. Augur, The struggle to keep scaling BEOL, and what we can do next, IEEE International Electronic Device Meeting (IEDM) (2016).
- [4] C. Schmidt, *et al*, Use of 3D X-Ray Microscopy for BEOL and Advanced Packaging Failure Analysis, International Symposium for Testing and Failure Analysis (ISTFA), (2017).
- [5] C. Schmidt, *et al*, Novel sample preparation and High-Resolution X-ray tomography for Package FA, International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), (2017).

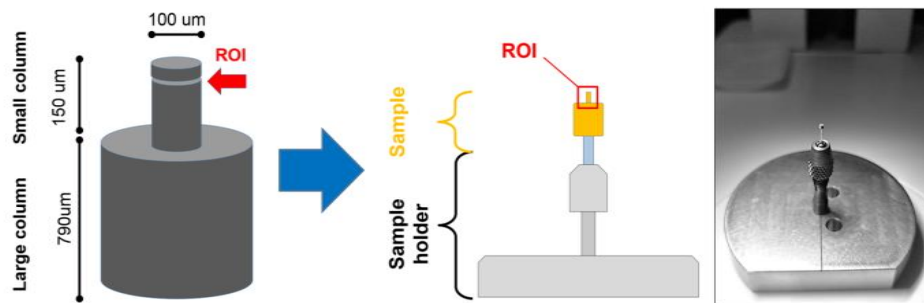


Figure 1. Schematic illustration of ROI-extraction from device under test and fixture on sample holder for XRM measurement.

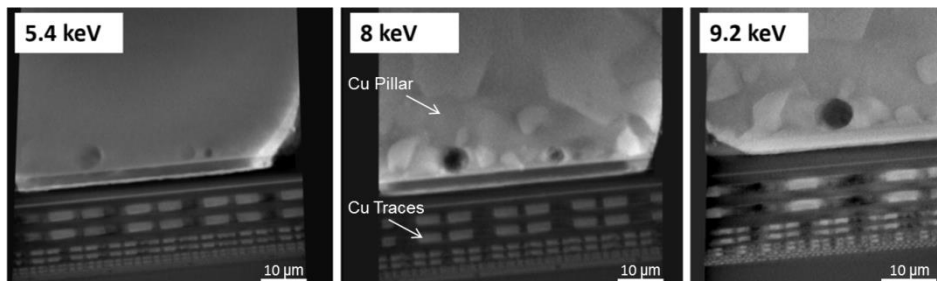


Figure 2. Virtual slice extracted from 3D XRM data set of BEOL/CPI inspection. The side-by side comparison compares the resulting feature visibility at different X-Ray energies.