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Compact three-way planar power divider with a simple structure

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Research Paper

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Abstract

A simple and compact three-way planar power divider, which avoids the floating common node of the isolation resistors, is presented. The proposed structure exhibits a wideband operation (measured frequency range of 1.6–3.3 GHz and bandwidth of 69.4%) with good return loss and isolation characteristics. Transmission line theory is used for the mathematical analysis and extraction of design equations, followed by simulations and experimental measurements that confirm the predicted results. The proposed divider achieves an equal power split (∼32%, -4.9 ± 0.4 dB insertion loss) between the input and each output port. The measured return loss is better than −10 dB at all ports, and the measured maximum isolation is close to −30 dB. The proposed design exhibits a fully planar structure, thus eliminating the need for a floating common node for the isolation resistors. Additionally, its structure is much simpler (i.e., no coupled lines, crossovers, or lumped capacitors are required) than other designs, achieves wideband operation, and provides design simplicity, flexibility, and easy implementation. Despite its simple noncomplicated structure, the proposed three-way planar divider achieves similar (or in some cases, better) performance and size than other more complicated structures. Furthermore, it can be expanded to an n-way structure.

Introduction

Multi-way power dividers are key components in many microwave applications such as power and low-noise amplifiers as well as phased antenna arrays [1–3]. In recent years, there has been an increasing demand for low-cost, compact, and miniaturized power dividers for various microwave and mm-wave applications. For this purpose, Wilkinson-type [4] and Gysel-type dividers [5] are widely used. Generally, an n-way Wilkinson divider is nonplanar for $n \geq 3$ because the 3D floating common node makes its planar implementation difficult. Although several planar structures have been proposed, they are rather complicated since they employ multi-section lines [6], p-i-n diodes [7], a multilayer structure [8], and coupled lines [9, 10]. Miniaturized planar structures have also been proposed, but they are also complicated because they either employ cascaded Lange couplers [11] or multi-section lines [12]. Recently, high-isolation planar dividers based on a recombinant structure and multi-section impedance transformers have been presented [13, 14]. In [15], a very simple wideband planar structure with good return loss and isolation characteristics was proposed. However, this structure was analyzed using only $\lambda/4$ lines, resulting in a $3\lambda/4$-long structure. More recent planar structures have been reported, but they are rather complicated since they employ composite right- and left-handed transmission lines with lumped capacitors [16] or provide only two-way power division [17].

In this work, we extend the work presented in [15] by investigating the design of a simple, wideband, and compact planar power divider with an arbitrary line length. It is demonstrated that the proposed structure can sufficiently operate using $\lambda/8$ lines, resulting in an overall length of $3\lambda/8$, which is half of that reported in [15]. The proposed design achieves a wideband operation (1.6–3.3 GHz) and can be expanded to an n-way structure. It also uses practical characteristic impedance values (thus providing easy implementation) and offers design flexibility. The proposed planar divider is first theoretically analyzed using transmission line theory and then fabricated on a microstrip substrate. Finally, experimental measurements are performed to validate the theoretically predicted results.

Circuit analysis

The proposed three-way planar power divider is presented in Fig. 1. It features a main block (shown as BLOCK), which consists of three transmission lines (each with characteristic impedance Z_1). All lines have an arbitrary electrical length θ ($0^\circ \leq \theta \leq 90^\circ$)

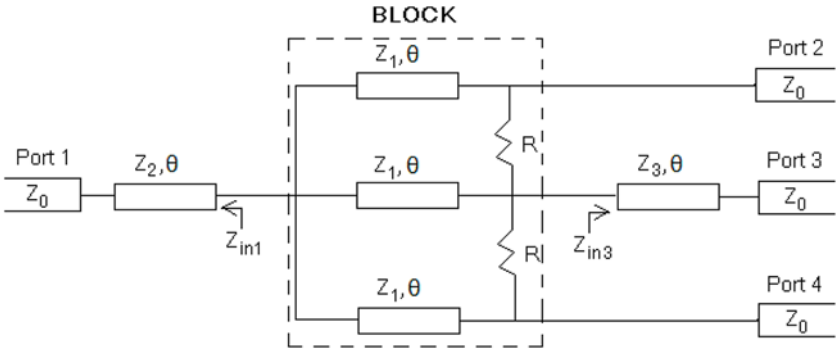

Figure 1. The proposed three-way wideband planar power divider employing transmission lines of arbitrary length θ.

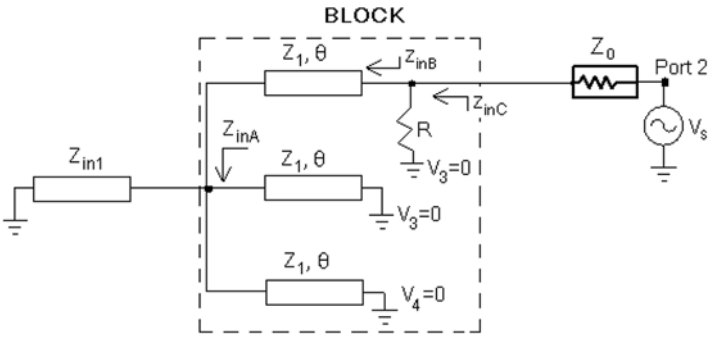

Figure 2. The circuit derived from the BLOCK (shown in Figure 1) by applying a voltage at port 2.

at the midpoint frequency of operation. The divider also employs two isolation resistors (each with value R) placed between ports 2 and 3 and between ports 3 and 4, respectively.

The extra transmission lines with characteristic impedances Z_2 and Z_3 and length θ at the input (port 1) and output (port 3), respectively, achieve the wideband characteristics of the proposed power divider. In this work, we set $\theta = 45^\circ$ to achieve a compact design. If we increase θ to 90°, the bandwidth will be increased but not significantly. However, this increase in θ leads to an increase in the total length of the divider, as reported in [15]. On the other hand, if we make $\theta < 45^\circ$ to achieve a more compact design, the bandwidth will be decreased to some extent and the lines will become very short, leading to coupling effects and difficulties in implementation.

Equal power splitting is achieved by employing transmission lines with the same characteristic impedance Z_1 inside the BLOCK (Fig. 1). The input and output lines with characteristic impedances Z_2 and Z_3, respectively, also achieve impedance matching. The derived equations for the input impedances Z_{inC} and Z'_{inC} (see Fig. 1) are set equal to Z_0 and Z_{in3}, respectively, by imposing the matching condition at ports 2 and 3, as shown in equations (9) and (16).

The input impedances Z_{in1} and Z_{in3} are given as follows:

$$Z_{\text{in1}} = Z_2 \frac{Z_0 + jZ_2 \tan\theta}{Z_2 + jZ_0 \tan\theta}, \tag{1}$$

$$Z_{\text{in3}} = Z_3 \frac{Z_0 + jZ_3 \tan\theta}{Z_3 + jZ_0 \tan\theta}. \tag{2}$$

Considering the components contained in the BLOCK (see Fig. 1), we initially apply a voltage source to port 2. Assuming ideal isolation at the remaining output ports, the voltages at ports 3 and 4 must be zero (i.e., $V_3 = V_4 = 0$). Therefore, from the BLOCK shown in Fig. 1, the circuit shown in Fig. 2 can be derived.

Based on Fig. 2, $Z_{\text{in}A}$ can be calculated as follows:

$$\frac{1}{Z_{\text{in}A}} = \frac{1}{Z_{\text{in1}}} + \frac{1}{jZ_1 \tan\theta} + \frac{1}{jZ_1 \tan\theta},$$

which results in the following equation:

$$Z_{\text{in}A} = \frac{Z_{\text{in1}} \cdot jZ_1 \tan\theta}{jZ_1 \tan\theta + 2Z_{\text{in1}}}. \tag{3}$$

In equation (3), by substituting Z_{in1} from equation (1), the following equation can be obtained:

$$Z_{\text{in}A} = \frac{jZ_0Z_1Z_2 \tan\theta - Z_1{Z_2}^2 \tan^2\theta}{jZ_1Z_2 \tan\theta - Z_0Z_1 \tan^2\theta + 2Z_0Z_2 + j2{Z_2}^2 \tan\theta}. \tag{4}$$

Also, based on Fig. 2, the input impedance $Z_{\text{in}B}$ can be written as follows:

$$Z_{\text{in}B} = Z_1 \frac{Z_{\text{in}A} + jZ_1 \tan\theta}{Z_1 + jZ_{\text{in}A} \tan\theta}. \tag{5}$$

In equation (5), by substituting $Z_{\text{in}A}$ from equation (4), the following equation can be obtained:

$$Z_{\text{in}B} = \frac{jZ_{\text{in1}}Z_1 \tan\theta - {Z_1}^2 \tan^2\theta + j2Z_1Z_{\text{in1}} \tan\theta}{jZ_1 \tan\theta + 2Z_{\text{in1}} - Z_{\text{in1}} \tan^2\theta}. \tag{6}$$

Furthermore, based on Fig. 2, the input impedance $Z_{\text{in}C}$ can be written as follows:

$$Z_{\text{in}C} = \frac{R \cdot Z_{\text{in}B}}{R + Z_{\text{in}B}}. \tag{7}$$

In equation (7), by substituting $Z_{\text{in}B}$ from equation (6), the following equation can be obtained:

$$Z_{inC} = \frac{R\left[j3Z_1Z_2 \tan\theta \cdot \frac{Z_0 + jZ_2 \tan\theta}{Z_2 + jZ_0 \tan\theta} - Z_1^2 \tan^2\theta\right]}{R\left[jZ_1 \tan\theta + Z_2 \frac{Z_0 + jZ_2 \tan\theta}{Z_2 + jZ_0 \tan\theta} \cdot (2 - \tan^2\theta)\right] + \left[j3Z_1Z_2 \tan\theta \frac{Z_0 + jZ_2 \tan\theta}{Z_2 + jZ_0 \tan\theta} - Z_1^2 \tan^2\theta\right]}. \tag{8}$$

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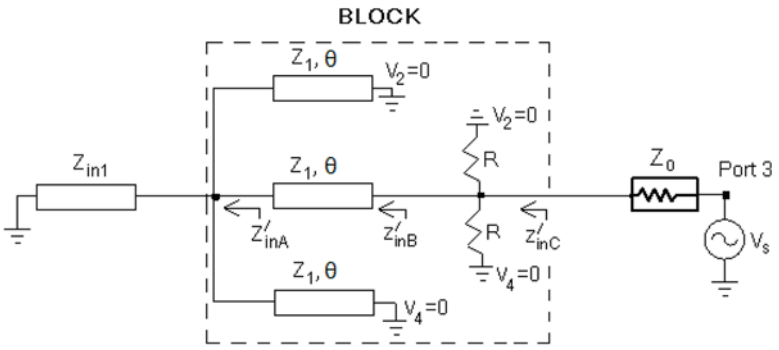

Figure 3. Circuit derived from the BLOCK (shown in Figure 1) when applying a voltage at port 3.

Table 1. Electrical parameter values for the proposed power divider in Figure 1

Z_0 (Ohm)	Z_1 (Ohm)	θ (degrees)	R (Ohm)	Z_2 (Ohm)	Z_3 (Ohm)
50	90	45	100	23.23	47.91

The above equation can also be derived if a voltage source is applied to port 4 because the divider of Fig. 1 is symmetric along its central axis.

The matching condition at port 2 requires

$$Z_{\text{in}C} = Z_0. \tag{9}$$

Next, we apply a voltage source to port 3. Assuming ideal isolation at the remaining output ports, the voltages at ports 2 and 4 must be zero (i.e., $V_2 = V_4 = 0$). Therefore, from the BLOCK shown in Fig. 1, the circuit shown in Fig. 3 can be derived.

Based on Fig. 3, $Z'_{\text{in}A}$ can be calculated as follows:

$$\frac{1}{Z'_{\text{in}A}} = \frac{1}{Z_{\text{in1}}} + \frac{1}{jZ_1 \tan\theta} + \frac{1}{jZ_1 \tan\theta},$$

which results in the following equation:

$$Z'_{\text{in}A} = \frac{Z_{in1} \cdot jZ_1 \tan\theta}{jZ_1 \tan\theta + 2Z_{\text{in1}}} \tag{10}$$

In equation (10), by substituting Z_{in1} from equation (1), the following equation can be obtained:

$$Z'_{\text{in}A} = \frac{jZ_1Z_2 \tan\theta \cdot (Z_0 + jZ_2 \tan\theta)}{jZ_1 \tan\theta \cdot (Z_2 + jZ_0 \tan\theta) + 2Z_2 \cdot (Z_0 + jZ_2 \tan\theta)}. \tag{11}$$

Also, based on Fig. 3, the input impedance $Z'_{\text{in}B}$ can be written as follows:

$$Z'_{\text{in}B} = Z_1 \frac{Z'_{\text{in}A} + jZ_1 \tan\theta}{Z_1 + jZ'_{\text{in}A} \tan\theta}. \tag{12}$$

In equation (12), by substituting $Z'_{\text{in}A}$ from equation (10), the following equation can be obtained:

$$Z'_{\text{in}B} = Z_1 \frac{\begin{array}{c}-3Z_1Z_2^2 \tan^2\theta - Z_1^2Z_2 \tan^2\theta + jZ_0Z_1Z_2 \tan\theta \\ -jZ_0Z_1^2 \tan^3\theta + j2Z_0Z_1Z_2 \tan\theta\end{array}}{\begin{array}{c}-Z_0Z_1^2 \tan^2\theta + 2Z_0Z_1Z_2 - Z_0Z_1Z_2 \tan^2\theta \\ +jZ_1^2Z_2 \tan\theta + j2Z_1Z_2^2 \tan\theta - jZ_1Z_2^2 \tan^3\theta\end{array}}. \tag{13}$$

Furthermore, based on Fig. 3, the input impedance $Z'_{\text{in}C}$ can be written as follows:

$$Z'_{\text{in}C} = \frac{RZ'_{\text{in}B}}{R + 2Z'_{\text{in}B}}. \tag{14}$$

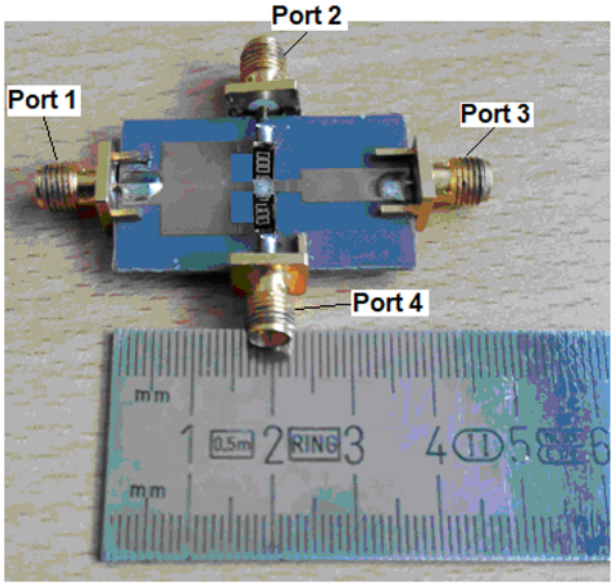

Figure 4. Fabricated PCB of the proposed power divider.

In equation (14), by substituting $Z'_{\text{in}B}$ from equation (12), the following equation can be obtained:

$$Z'_{\text{in}C} = \frac{\begin{array}{c}RZ_1\left(-3Z_1Z_2^2 \tan^2\theta - Z_1^2Z_2 \tan^2\theta + jZ_0Z_1Z_2 \tan\theta\right. \\ \left.-jZ_0Z_1^2 \tan^3\theta + j2Z_0Z_1Z_2 \tan\theta\right)\end{array}}{\begin{array}{c}R\left(-Z_0Z_1^2 \tan^2\theta + 2Z_0Z_1Z_2 - Z_0Z_1Z_2 \tan^2\theta\right. \\ \left.+jZ_1^2Z_2 \tan\theta + j2Z_1Z_2^2 \tan\theta - jZ_1Z_2^2 \tan^3\theta\right) \\ +2Z_1\left(-3Z_1Z_2^2 \tan^2\theta - Z_1^2Z_2 \tan^2\theta + jZ_0Z_1Z_2 \tan\theta\right. \\ \left.-jZ_0Z_1^2 \tan^3\theta + j2Z_0Z_1Z_2 \tan\theta\right).\end{array}} \tag{15}$$

The matching condition at port 2 requires

$$Z'_{\text{in}C} = Z_{\text{in3}}. \tag{16}$$

Implementation, results, and discussion

Equations (8), (9) and (15), (16) can be used as the design equations of the proposed power divider. These equations are satisfied for a number of solutions. Thus, the variety of parameter values provides design flexibility. To achieve a compact design, $\theta = 45°$ was selected at a midpoint frequency of 3 GHz. Also, by selecting $Z_0 = 50$ Ohm, $R = 100$ Ohm, and $Z_1 = 90$ Ohm,

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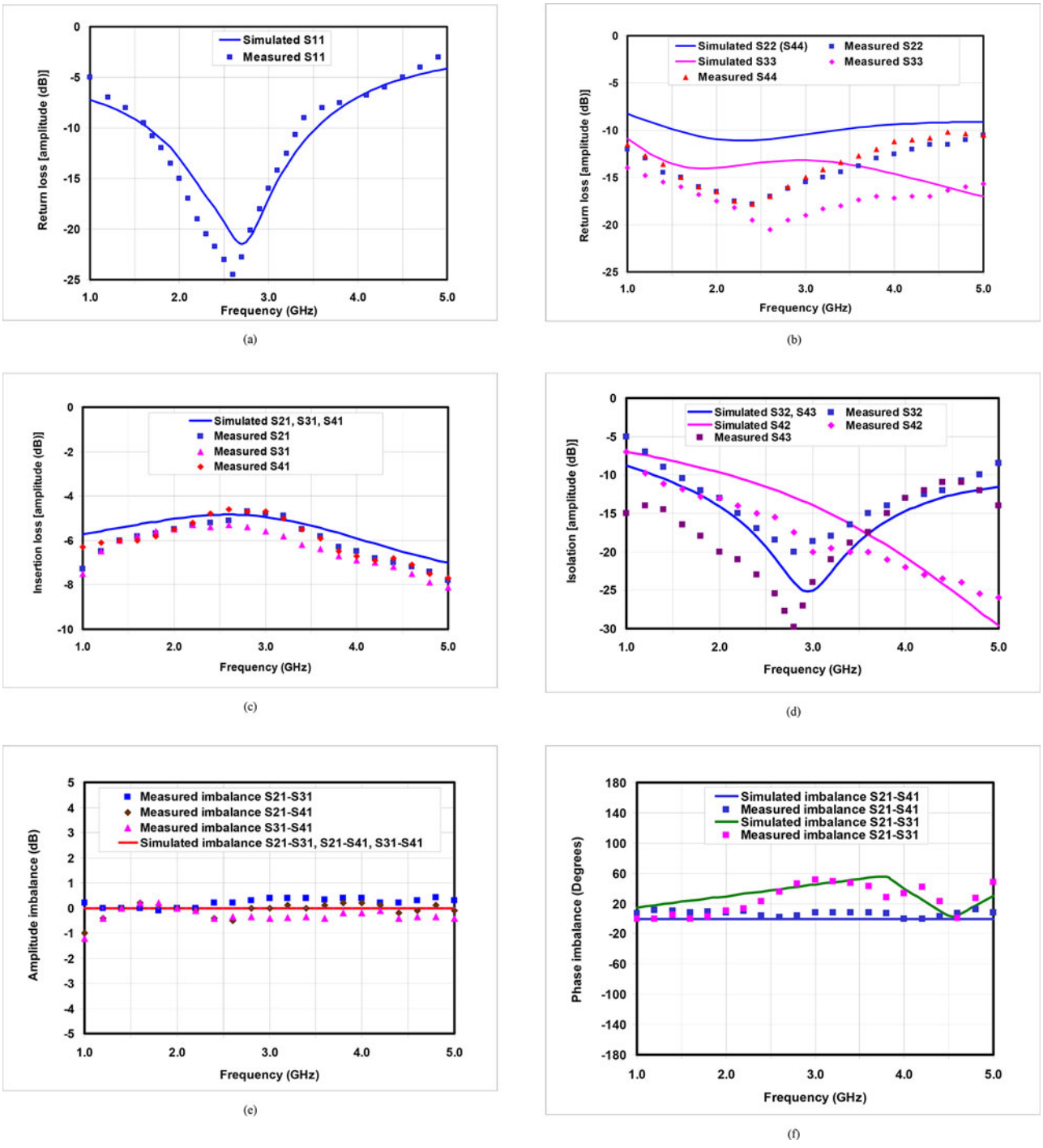

Figure 5. Measured results for (a) input return loss, (b) output return loss, (c) insertion loss, (d) port isolation, (e) amplitude imbalance, and (f) phase imbalance of the proposed three-way planar divider shown in Figure 1

equations (8), (9) and (15), (16) yield practically realizable impedance values ($Z_2 = 23.23$ Ohm and $Z_3 = 47.91$ Ohm). These parameter values are summarized in Table 1.

The proposed three-way wideband planar power divider shown in Fig. 1 was fabricated on a printed circuit board (PCB) using a TACONIC substrate with a typical dielectric constant of 2.2 (Fig. 4). The layout of the proposed power divider was produced using the Advanced Design System simulation software. Then, we placed a mask of the layout on the top copper surface of the TACONIC substrate and immersed it into a solution of sodium hydroxide to remove the unwanted copper. Thus, the upper conductors of the microstrip lines with the desired dimensions were fabricated. Commercial 100-Ohm resistors were used to achieve the necessary isolation between the output ports. These resistors could, in principle, cause some parasitic effects. However, in the operating frequency range of the divider, these effects are negligible. We employed an Agilent E5071C vector network analyzer to measure the scattering parameters (amplitude and phase) of the

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Table 2. Performance comparison of the proposed structure with the performance of previously published works

Ref.	Design structure	Return loss (dB)	Insertion loss (dB)	Max. isolation (dB)
[8]	Three-way, narrow-coupled lines, slotted ground plane, lumped capacitors	<−16	−4.77	−17
[9]	Three-way, narrow-coupled lines	<−10	−4.80	−19
[11]	Three-way, inner-layer crossovers, Lange couplers (operation at <0.8 GHz)	<−20	−5.10	−35
[13]	Three-way planar	<−10	−4.99	−30
[14]	Three-way planar	<−10	−4.99	−31
[15]	Three-way planar	<−13	−4.60	−20
[16]	Eight-way planar, composite right- and left-handed transmission line, hybrid coplanar waveguide microstrip line, lumped capacitors	<−15	−9.20	−40
[17]	Two-way planar	<−11	−3.00	−15
This work	Three-way planar	<−10	−4.90	−30

Ref.	Maximum amplitude imbalance (dB)	Maximum phase imbalance (degrees)	Fractional bandwidth (%)	Overall size
[8]	2.00	Not mentioned	97.8	$0.86\lambda \times 0.86\lambda$
[9]	0.20	Not mentioned	96.0	$0.59\lambda \times 0.38\lambda$
[11]	1.20	90	42.7	$0.54\lambda \times 0.10\lambda$
[13]	2.00	Not mentioned	34.8	$0.26\lambda \times 0.31\lambda$
[14]	2.00	8	43.5	$0.27\lambda \times 0.34\lambda$
[15]	0.40	Not mentioned	66.7	$0.75\lambda \times 0.37\lambda$
[16]	0.24	∼5	36.4	$0.25\lambda \times 0.27\lambda$
[17]	0.50	Not mentioned	52.6	$0.32\lambda \times 0.20\lambda$
This work	0.80	∼51	69.4	$0.38\lambda \times 0.26\lambda$

fabricated PCB over the frequency range 1–5 GHz. Before conducting measurements, we performed the standard transmission–line–through calibration procedure. The graphs in Fig. 5 show the simulated and experimental responses of the proposed divider. Good agreement can be observed. The discrepancies are mainly due to the limited accuracy of the etching process and the effect of the connectors, which were not included in the simulation. Due to our limited lab resources, we could not perform any calibration or correction procedures to address the discrepancies caused by the etching process and connectors during the measurement process. It is evident that in the frequency range 1.6–3.3 GHz (a fractional bandwidth of $\frac{3.3-1.6}{2.45} \cong 69.4\%$), the proposed divider achieves equal power split (∼32%, -4.9 ± 0.4 dB insertion loss) between the input and each output port and good matching and isolation characteristics. The measured return loss is better than −10 dB at all ports, and the measured maximum isolation is close to −30 dB. The maximum measured amplitude imbalance is ∼0.8 dB. The maximum measured phase imbalance between ports 2 and 4 is ∼8 degrees, whereas that between ports 2 and 3 (or 4 and 3) is ∼51 degrees. This is due to the extra length θ of the line with characteristic impedance Z_3 shown in Fig. 1.

Generally, the phase imbalances measured are not significant in applications requiring an accurate splitting ratio. However, the phase imbalances measured between certain ports, although acceptable, may have an impact in phase array applications. In cases requiring very small phase imbalances, an appropriate phase shifter could be used.

A performance comparison of the proposed planar power divider with the performance of previously published designs is shown in Table 2. It is evident that the performance of the proposed design is better than the performance of most other designs in terms of insertion loss, isolation, bandwidth, and size but falls short in terms of return loss. However, its design flexibility, easy implementation, and expansion to an *n*-way structure make it an attractive proposition.

Conclusion

In this work, a planar three-way wideband power divider that avoids the floating common node of the isolation resistors was designed, simulated, fabricated, and tested. The mathematical analysis and extraction of design equations were based on the transmission line theory. The divider was fabricated on a microstrip substrate. Measured results showed a good agreement with the predicted data. It was also demonstrated that despite its very simple noncomplicated structure, the proposed design achieves similar performance and size compared with other more complicated structures. Furthermore, it provides design flexibility, can be easily implemented, and can be expanded to an *n*-way structure.

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Competing interests. The authors declare no conflict of interests.

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