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Direct Detectors of Electrons for STEM and TEM

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At our request, the Instrumentation Division at BNL is developing two new electron detectors based on direct conversion of the incident energy into electron-hole pairs in silicon (1 electron-hole pair per 3.6 eV deposited). These offer high quantum efficiency, fast direct pixel readout, and resistance to radiation damage due to exclusion of oxides from active regions.

The first detector is intended for STEM, where the detector plane contains a CBED (convergent beam electron diffraction) pattern that gives information about the spatial packing of atoms in the path of the probe [1]. The normal STEM detectors integrate over annular ranges, discarding the detailed distribution in order to give averages that can be read out at the scanning speed of 1-30 μsec/pixel.

The STEM detector [2] version 2 completed in Feb. 05 uses high resistivity silicon 300 microns thick and fully depleted in order to convert all the energy in a 40 keV incident electron into roughly 10,000 electron-hole pairs. Since the readout noise is only 300 electron-hole pair equivalents, the charge measurement effectively counts the number of individual incident electrons. The electronics saturates at about 36,000 electron-hole pairs, producing a dynamic range of 32 incident electrons per pixel. The 180x180 micron pixels are arranged in a 32x32 array. Each pixel contains a switching transistor connecting one of the 32 pixels in a row directly to one of the 32 readout lines with a readout time of a few μsec. With 32 independent outputs through the vacuum chamber, the entire array can be read in less than 100 μsec. The production of the STEM detector involves 157 separate steps and the first run had poor contacts to the readout transistor. The second run is now being tested. Larger arrays up to 128x128 elements are available on the same wafer and will be tested if needed. Performance could be enhanced significantly by moving the readout preamp inside the vacuum system and increasing the multiplexing of the output signals. Increasing the number of recorded signals from the current 5 to over 1000 will place significant additional demands on the data acquisition computer, but this is still within the capability of current PC technology. Image simulation is being used to generate artificial data to test reconstruction algorithms, as well as refine the design parameters.

The second detector under development is intended for TEM and is in the design stage. It would use current CMOS technology to give an array of 1024x1024 pixels with single electron counting, integration of up to 64,000 counts per pixel (16-bits) and fast readout (up to 1000 frames per sec). This standard CMOS process incorporates an epilayer 8-12 microns thick where incident electrons generate signal charge. Since the intended electron energy is 200 keV, the thin layers above the epilayer will not attenuate the beam significantly and the thinness of the epilayer will reduce broadening of the beam, while still providing adequate signal for single electron detection. A major limitation of the use of high resistivity silicon in the STEM detector described above is that only n-type transistors can be used in the design. This is not a problem with the commercial process, making it possible to include a 16-bit scalar within each pixel. The major challenge in the design is to channel the signal electrons away from the remainder of the electronics. This is done by placing electrodes in strategic positions both as shields and as a way to speed up collection of the charge. In the case shown in Fig. 2, the collection time is roughly 5 nsec.

This detector should be useful for both imaging and diffraction in TEM. It will be particularly attractive for low-dose imaging and tomography.

References

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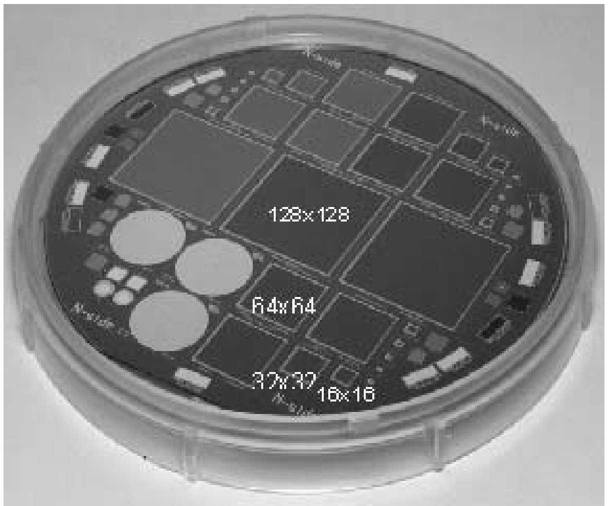

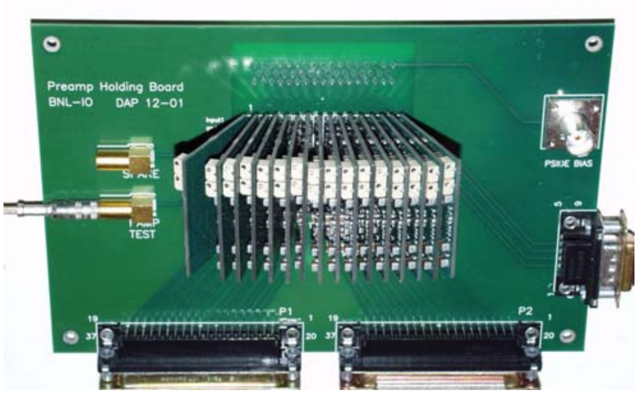

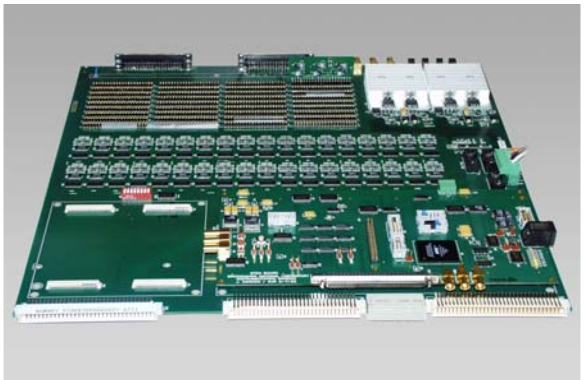

Fig. 1. Wafer containing several STEM detectors of various sizes, preamp board and DSP board.

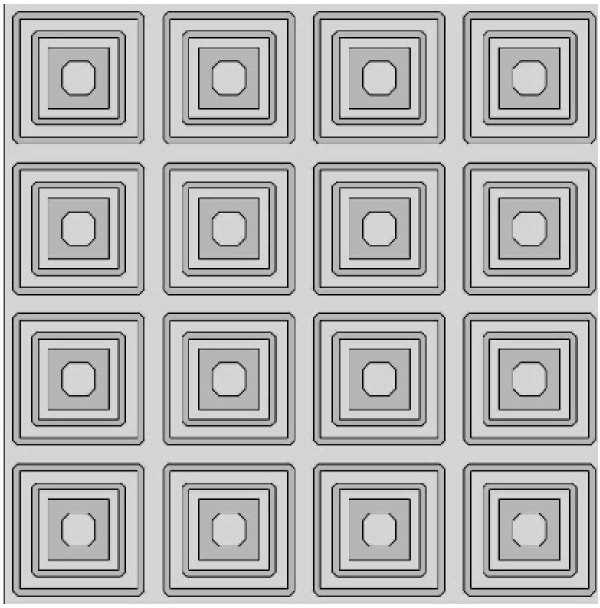

Fig. 2 Mask layout for pixels in the TEM detector.