DESIGN AND FABRICATION OF LARGE CCDs FOR THE KECK OBSERVATORY DEIMOS SPECTROGRAPH

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ABSTRACT: The Keck II Deep Imaging Multi-Object Spectrograph (DEIMOS) is a general purpose, faint object, multi-slit, double-beam spectrograph which offers wide spectral coverage, high spectral resolution, high throughput, and long slit length on the sky. This powerful instrument will be the principal optical spectrograph on the Keck II telescope. DEIMOS is optimized for faint-object spectroscopy of individual point sources, low-surface-brightness extended objects, or widely distributed samples of faint objects on the sky. To obtain high resolution (~ 1 Å) and wide spectral coverage (up to 5000 Å) the spectrograph uses wide angle cameras and large CCD detectors with many pixels.

This paper describes some of the work being carried out to obtain the CCD detectors required for the DEIMOS spectrograph. In addition, results are presented on the fabrication and characterization of a 4k x 2k three-side buttable CCD produced by Orbit Semiconductor, a silicon foundry in San Jose, California. This CCD was fabricated to test the ability of Orbit to produce high quality scientific CCDs with the characteristics required for detectors to be used in DEIMOS and other optical instruments of the Keck Observatory.

1. THE DETECTORS

Light entering the DEIMOS spectrograph through a slit mask strikes a single collimator, and is then divided into two beams by a V-shaped "tent" mirror. After striking a grating (or flat mirror in direct-imaging mode), each beam enters a wide-angle camera and is imaged onto a large detector mosaic. Each mosaic will be 8k x 8K pixels consisting of eight 4k x 2k detectors with 15 μm pixels. The details of the DEIMOS spectrograph design will be presented at other conferences. Here we focus only on the detectors.

A mosaic of CCDs is required for DEIMOS since an 8k x 8k array of 15 μm pixels can not be produced in a single, monolithic CCD with current CCD fabrication facilities anywhere. On a 100 mm silicon wafer a 4k x 4k CCD can be produced. However, for this application we chose a 4k x 2k format because of the higher fabrication yield likely with the smaller device. To form the large mosaic the devices must be three-side buttable, with a single serial register along a short edge. The spectrum runs in the long dimension of the CCDs and we want to minimize spectral loss in the gaps between CCDs. Therefore, our goal is to have no more than a 200 μm gap along the top edge of the CCDs. Along the other sides (the 4k-long edge) we

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want to have no more than a 1000 μm gap. The spectrograph design is making good use of the dead areas in the focal plane created by these wider gaps by placing there the mechanical members that define the shape of the slit mask. Table 1 lists some of the specifications for the CCDs.

TABLE 1

Specifications for CCDs

Geometry	2048 x 4096 15 μm pixels
	Three-edge abuttable with serial along short edge
	Dead region < 100 μm on top (2048) edge
	< 500 μm on 4096 edge
	Flatness: $\pm$5 μm at -100° C
	Thinned to approx. 15 μm (assuming standard epitaxial wafers)
Mosaic	Each CCD to be individually packaged so they can be inserted and removed from a larger mosaic
	Gaps: < 200 μm on top and < 1000 μm on edges
Flatness	Entire mosaic maintains $\pm$5 μm spec.
Amplifier	Readout noise < 5 e^- (2 e^- preferred) at 100 k pixels/sec
Linearity	< 5% deviation over full dynamic range of the CCD
RQE	> 60% at 350 nm (goal)
	> 90% peak RQE somewhere in the range 500 - 700 nm
	> 50% at 900 nm
	> 15% at 1000 nm (goal)
	< 5% variation over entire CCD
	< Stable RQE
Charge	CTE > 0.99999 for 1600 e^- signals
	Nor more than 100 pixels that exhibit low level CTE problems
	Full well > 150,000 e^-
	Dark current < 0.005 e^-/sec at -100° C
Fringing	Monochromatic interference fringing amplitude < 10% peak-to-peak

2. CCD FABRICATION

The CCDs described in Table 1 do not yet exist, yet are vital if DEIMOS is to achieve its full scientific potential. For this reason we can not just wait to see if they become available. We must do everything we can within our budget limitations to try to make sure they become available. Keck Observatory has chosen to work on several fronts. On one front, Keck is looking for a "full service" vendor who can supply us completed, working devices. A survey of potential suppliers identified MIT/Lincoln National Laboratory as the best candidate who could fabricate the CCDs at reasonable cost, and with a reasonable expectation of success within the time frame of the DEIMOS project. Lincoln has demonstrated capabilities in CCD

mosaics, thinned CCDs, flat CCDs, and very low readout noise. To develop the Lincoln potential an international consortium has been established to fund a one year engineering effort at approximately $500 K total investment. This consortium is coordinated by Gerard Luppino of the University of Hawaii.

On a second front, Keck is actively funding the development of the 4k x 2k CCD through foundry sources. If we can acquire the CCDs we need through foundry sources, the total cost for the large number of devices we need could be significantly less than the cost from a "full service" vendor. With the eventual disruption of the Loral, Newport Beach facilities in mind, we began to look for an alternative foundry. At the same time, Orbit Semiconductor, a major silicon foundry, approached us and proposed a collaborative development effort, which would help them develop their scientific CCD capabilities. As an ambitious first test of their CCD fabrication abilities we decided to design a 100 mm wafer with one 4k x 2k CCD and two 2k x 2k CCDs. The remainder of this paper describes some of the results from these first wafer runs. As we will show, the devices produced by Orbit are very high quality scientific CCD imagers.

The design of the 4k x 2k CCD was done with the requirement of the DEIMOS CCDs in mind. The buttability requirement was met, with a dead space of about 200 μm between the saw blade line and the edge of the imaging area, in the long dimension of the device, and dead space of about 45 μm from the saw line to the imaging area along the top of the device. The design also includes split serial clocking, with identical amplifiers at each end of the horizontal shift register, which is located along the bottom of the device. MPP and notch implant technologies are also used to reduce dark current and improve charge transfer efficiency (CTE) respectively.

After fabrication the wafers were tested for DC shorts at Orbit and then delivered to Lick Observatory where we performed a detailed wafer probe examination of all working devices. After evaluating the devices on the wafer, we selected an engineering grade 4k x 2k device (device #464-12) for our initial lab tests. The wafer was diced, and then glued with Epo-Tek 301-2 epoxy to a piece of Kovar and subsequently electrically wire-bonded to a small printed circuit board.

3. PERFORMANCE CHARACTERISTICS

We performed all of the tests in a liquid nitrogen-cooled dewar. Our electronics includes a 20 x gain preamplifier located outside the dewar, and a correlated-double-sampling amplifier with 16 s sample times. The CCD was cooled to 120° C for all tests. Our measured performance characteristics for device 464-12 are summarized in Table 2, and discussed briefly in the following paragraphs.

3.1 Dark Current

Dark current, due to thermally generated electrons, is a limitation on read noise performance and is therefore an important parameter in astronomical applications where signal

TABLE 2

Measured Performance for an Orbit 4k x 2k CCD

4k x 2k CCD 464-12 Measured Performance	
Read Noise	< 4 electrons
Dark Current	<< 0.001 e^-/pixel/sec (MPP mode)
Horizontal CTE	> 0.999997 per phase (see Fig. 1)
Full Well (MPP)	70,000 e^-, (non MPP): 170,000 e^-
Low level localized traps	59 total (see Fig. 2)
RQE	Typical thick CCD response (see Fig. 3)

levels may be very low. In a 1000 second dark integration we found an average dark current of < 1 e^- when the device was operated with MPP clocks. In fact, further tests with much longer integrations will be necessary before we can reliably determine just how low the dark current is. Spurious charge generated by running the vertical clocks can be reduced to a negligible level by setting the vertical clock levels to +two volts and -six volts.

3.2 Read Noise

Read noise places a lower limit on the smallest charge packets that can be detected and measured by the CCD. For low light level observations, the read noise value becomes a very important value in determining the CCD's limitations. To measure the read noise we clock the serial register so that any charge is transferred away from the output amplifier. All other signal processing is the same. With 16 s amplifier sample times the read noise per pixel was 3.5 e^-. (The intrinsic noise of our system with input grounded is less the 1 e^-.) We hope to maintain this noise figure, while increasing our readout speed, by incorporating the first stage of the preamplifier on the CCD package.

3.3 CTE

To measure charge transfer efficiency we illuminate the CCD with an Fe-55 x-ray source, each absorbed x-ray generating 1620 electrons. By comparing the measured charge packet with the expected charge packet the CTE can be measured accurately. The plot to the right (Fig. 1) shows the distribution of observed events, as a function of column number. (Multiply the vertical axis by 1.4 to convert the digital numbers shown to electrons.) If all of the charge produced from each absorbed X-ray were collected by a single pixel and if the CTE were perfect, then all of the events would fall on a single horizontal line in the figure. In fact, the charge from X-rays absorbed deep in the CCD may diffuse into two or more pixels so there are many more "split" events than single-pixel events. In the Figure the single pixel events fall on a (nearly) horizontal line at a level of about 1160. We fit a straight line to these events, and we measure the slope of the fitted line. The slope is a direct measure of the CTE, and for this

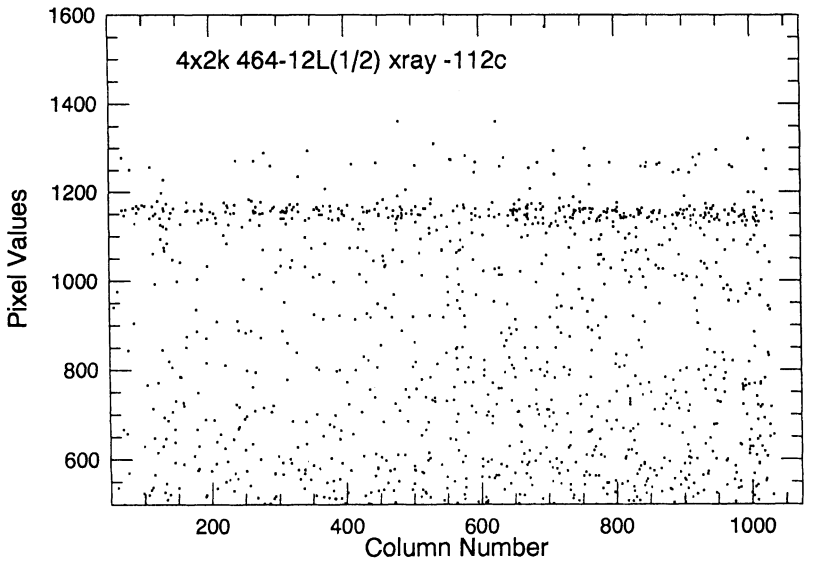

Fig. 1. CTE measured using Fe-55 X-rays

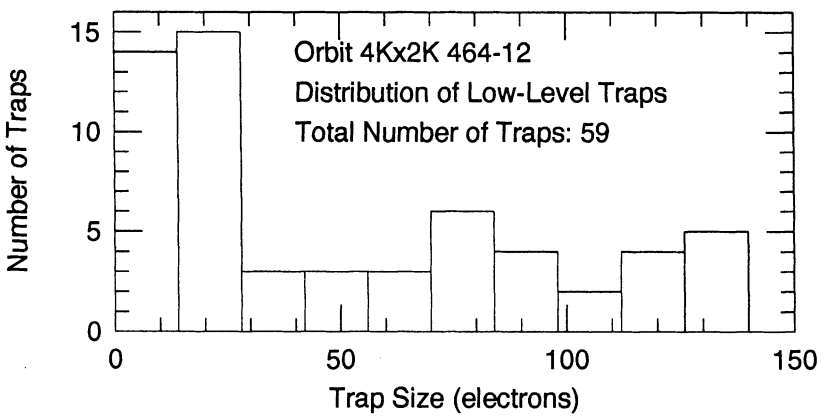

Fig. 2. Size Distribution of Localized Traps

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device we found a CTE of 0.999997 per phase.

3.4 Full Well

We measured the full well capacity of the CCD in MPP mode, with all vertical clocks inverted during integration, and in non-MPP mode, with one vertical clock held high during integration. The measured full well was 70,000 e^- in MPP mode and 170,000 e^- in non-MPP mode. Since several different MPP doping levels were tried on different wafers in this run, these results can't be taken as an indication of the "typical" full well. As we have the opportunity to measure more devices we will learn how doping levels effect full well capacity.

3.5 Localized Traps

We measure low-level traps by taking a uniform illumination exposure that results in about 300 e^- per pixel. Then, before reading out the image we shift the charge vertically on the CCD. First the charge is shifted in one direction by 24 rows and then is shifted back in the other direction by 24 rows. This is repeated 40 times before the image is read out. A low level trap shows up as a pixel with excess charge (where charge has been trapped on each shift) and one or more pixels with lower than expected charge (where the charge has been lost). The size of the trap is measured by dividing the size of the excess charge by the number of shifts. Fig. 2 shows the size distribution determined for the 4k x 2k CCD. There were a total of 59 traps located on the CCD by this method. This is an exceptionally small number of traps for such a large device. We found a consistent number of traps (about half) in the Orbit 2k x 2k CCDs we have measured.

3.6 RQE

We measured responsive quantum efficiency using a set of interference filters and a calibrated photodiode. Fig. 3 shows the measured RQE, which we find to be typical of thick CCDs.

4. CONCLUSIONS

The work being done with Lincoln Laboratory and Orbit Semiconductor represent an aggressive effort to produce the CCDs needed for the DEIMOS spectrograph. However, none of this work prevents Keck from considering other options, should they become available. For instance, it may be possible that SITe or some other full service vendor may develop an appropriate CCD, and it may be possible that one of Loral's other fabrication facilities may prove to be technically viable at reasonable cost. We will continue to monitor possibilities.

We began the project with Orbit Semiconductor as a test to see if they could produce the CCDs we need for the DEIMOS project. We still have some work to do, but our results show that Orbit can indeed produce very large, high quality scientific CCDs. The CCD mosaics for the DEIMOS spectrograph will have to be thinned, backside treated CCDs, and they will have to be maintained flat and co-planar to within about ten micrometers over the entire mosaic.

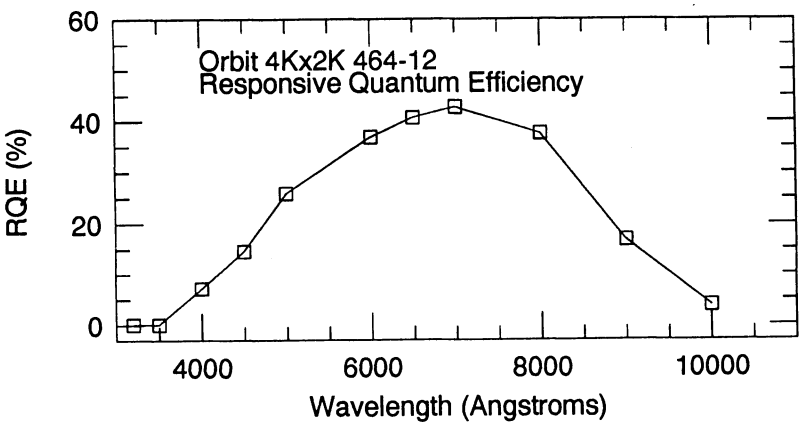

Fig. 3. Measured RQE for for thick 4k x 2k CCD

These requirements present formidable technical challenges which we are now beginning to address.

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DISCUSSION

PHILIP: What is the readout time of a 2k x 4k chip?

STOVER: This depends how many amplifiers are used and the integration time per pixel. with our current system, and reading only one amplifier it takes about four minutes. Our goal is to read much faster and to use both amplifiers. Other groups have reported problems reading multiple amplifiers. If we cannot read multiple amplifiers then low-noise high-speed readout becomes even more important.

COHEN: We are currently working hard on fixing the negative cross talk in the multi-amplifier readout electronics. We should have that completed within the next two months.

STOVER: Other groups have reported similar problems too.

QUESTION: Do your 10% fringing specifications refer to front-side or back-side illumination, and to what wavelength does it refer?

STOVER: It refers to back-side illumination and is the highest amplitude at any wavelength.

WALKER: Please comment on the yield of Orbit 2k x 4k devices obtained so far.

STOVER: We had five working 4k x 2k CCDs with only one really good device. After Orbit did our wafer runs they did several more on their own to try to improve yield. The next three wafer runs will show whether or not Orbit can provide these CCDs with reasonably high yield.

QUESTION: Will you have the facility to cold test the CCDs before thinning?

STOVER: Yes, we can cool the wafers to about -10° C to test them.

JORDEN: What is the Keck budget for CCDs? And what devices are to be provided for this money?

STOVER: Keck is spending about $100,000 US on the Lincoln Labs effort, $100,000 on the foundry effort and $100,000 on the CCD thinning effort. Once all of these development efforts are concluded there should be one to two million dollars for actual CCD acquisition. We need about 24 science grade devices.

McBREEN: What is the current situation with Loral producing large CCDs?

STOVER: Loral, Newport Beach has stopped taking orders. Further work may be possible at Loral's Milpitas facility. Loral has also purchased a fabrication facility from IBM. This facility uses 5-inch wafers, so larger CCDs or more CCDs per wafer may be possible. However, it is still not clear what the costs at either of these facilities may be. We may do some more work with Loral after these issues are resolved.

McBREEN: Are you considering large frame transfer CCDs?

STOVER: Yes, the Lincoln Lab CCDs will have frame transfer. This is being done to satisfy interests of some of the consortium members. However, the DEIMOS spectrograph does not use this feature, and since it will increase the gaps between the CCDs in a mosaic, frame transfer is not included in the orbit semiconductor design.